

Vijay Janapa Reddi

List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/4913759/publications.pdf>

Version: 2024-02-01

49
papers

5,296
citations

687363

13
h-index

713466

21
g-index

49
all docs

49
docs citations

49
times ranked

2431
citing authors

#	ARTICLE	IF	CITATIONS
1	Pin. , 2005, , .		2,213
2	Pin. ACM SIGPLAN Notices, 2005, 40, 190-200.	0.2	1,105
3	GPUWattch. , 2013, , .		358
4	MLPerf Inference Benchmark. , 2020, , .		180
5	Resilient Architecture Design for Voltage Variation. Synthesis Lectures on Computer Architecture, 2013, 8, 1-138.	1.3	164
6	GPUWattch. Computer Architecture News, 2013, 41, 487-498.	2.5	134
7	Mobile CPU's rise to power: Quantifying the impact of generational mobile CPU design trends on performance, energy, and user satisfaction. , 2016, , .		102
8	Deep Reinforcement Learning for Cyber Security. IEEE Transactions on Neural Networks and Learning Systems, 2023, 34, 3779-3795.	11.3	100
9	Voltage emergency prediction: Using signatures to reduce operating margins. , 2009, , .		86
10	Event-based scheduling for energy-efficient QoS (eQoS) in mobile Web applications. , 2015, , .		82
11	MLPerf: An Industry Standard Benchmark Suite for Machine Learning Performance. IEEE Micro, 2020, 40, 8-16.	1.8	76
12	Voltage Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software-Guided Thread Scheduling. , 2010, , .		73
13	High-performance and energy-efficient mobile web browsing on big/little systems. , 2013, , .		62
14	Safe limits on voltage reduction efficiency in GPUs. , 2015, , .		60
15	Adaptive guardband scheduling to improve system-level efficiency of the POWER7+. , 2015, , .		39
16	GPU voltage noise: Characterization and hierarchical smoothing of spatial and temporal voltage noise interference in GPU architectures. , 2015, , .		37
17	GPUVolt. , 2014, , .		29
18	Gables: A Roofline Model for Mobile SoCs. , 2019, , .		28

#	ARTICLE	IF	CITATIONS
19	An event-guided approach to reducing voltage noise in processors. , 2009, , .		25
20	Eliminating voltage emergencies via software-guided code transformations. Transactions on Architecture and Code Optimization, 2010, 7, 1-28.	2.0	22
21	Two Billion Devices and Counting. IEEE Micro, 2018, 38, 6-21.	1.8	22
22	Predicting Voltage Droops Using Recurring Program and Microarchitectural Event Activity. IEEE Micro, 2010, 30, 110-110.	1.8	21
23	Exceeding Conservative Limits: A Consolidated Analysis on Modern Hardware Margins. IEEE Transactions on Device and Materials Reliability, 2020, 20, 341-350.	2.0	21
24	Software-assisted hardware reliability. , 2009, , .		20
25	WebCore: Architectural support for mobile Web browsing. , 2014, , .		20
26	The Sky Is Not the Limit: A Visual Performance Model for Cyber-Physical Co-Design in Autonomous Machines. IEEE Computer Architecture Letters, 2020, 19, 38-42.	1.5	19
27	Voltage-Stacked GPUs: A Control Theory Driven Cross-Layer Solution for Practical Voltage Stacking in GPUs. , 2018, , .		18
28	A Survey on Machine Learning Accelerators and Evolutionary Hardware Platforms. IEEE Design and Test, 2022, 39, 91-116.	1.2	17
29	Ivory. , 2017, , .		16
30	Accelerating Robot Dynamics Gradients on a CPU, GPU, and FPGA. IEEE Robotics and Automation Letters, 2021, 6, 2335-2342.	5.1	16
31	Air Learning: a deep reinforcement learning gym for autonomous aerial robot visual navigation. Machine Learning, 2021, 110, 2501-2540.	5.4	15
32	WebCore. Computer Architecture News, 2014, 42, 541-552.	2.5	13
33	Robust and resilient designs from the bottom-up: Technology, CAD, circuit, and system issues. , 2012, , .		12
34	Simulation and Analysis Engine for Scale-Out Workloads. , 2016, , .		11
35	Robomorphic computing: a design methodology for domain-specific accelerators parameterized by robot morphology. , 2021, , .		11
36	Accelerator-level parallelism. Communications of the ACM, 2021, 64, 36-38.	4.5	10

#	ARTICLE	IF	CITATIONS
37	Resilient Architectures via Collaborative Design: Maximizing Commodity Processor Performance in the Presence of Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1429-1445.	2.7	9
38	Voltage-Stacked Power Delivery Systems: Reliability, Efficiency, and Power Management. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5142-5155.	2.7	8
39	Widening Access to Applied Machine Learning with TinyML. , 0, , .		8
40	Analyzing and Improving Fault Tolerance of Learning-Based Navigation Systems. , 2021, , .		6
41	Roofline Model for UAVs: A Bottleneck Analysis Tool for Onboard Compute Characterization of Autonomous Unmanned Aerial Vehicles. , 2022, , .		6
42	Predictive Guardbanding: Program-Driven Timing Margin Reduction for GPUs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 171-184.	2.7	5
43	GRiD: GPU-Accelerated Rigid Body Dynamics with Analytical Gradients. , 2022, , .		5
44	Persistence in dynamic code transformation systems. Computer Architecture News, 2005, 33, 69-74.	2.5	4
45	FARSI: An Early-stage Design Space Exploration Framework to Tame the Domain-specific System-on-chip Complexity. Transactions on Embedded Computing Systems, 2023, 22, 1-35.	2.9	4
46	Asymmetric Resilience for Accelerator-Rich Systems. IEEE Computer Architecture Letters, 2019, 18, 83-86.	1.5	2
47	Hardware and software co-design for robust and resilient execution. , 2012, , .		1
48	Efficient and Reliable Power Delivery in Voltage-Stacked Manycore System with Hybrid Charge-Recycling Regulators. , 2018, , .		1
49	Erratum to "Predictive Guardbanding: Program-Driven Timing Margin Reduction for GPUs" IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 1272-1272.	2.7	0