Simoen Eddy

List of Publications by Year
in descending order

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150 papers	2,021 citations	331259 21 h-index	344852 36 g-index
152 all docs	152 docs citations	152 times ranked	1497 citing authors

#	Article	IF	Citations
1	On the flicker noise in submicron silicon MOSFETs. Solid-State Electronics, 1999, 43, 865-882.	0.8	303
2	Challenges and opportunities in advanced Ge pMOSFETs. Materials Science in Semiconductor Processing, 2012, 15, 588-600.	1.9	72
3	Border Traps in Ge/IIIâ€“V Channel Devices: Analysis and Reliability Aspects. IEEE Transactions on Device and Materials Reliability, 2013, 13, 444-455.	1.5	70
4	Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature. IEEE Transactions on Electron Devices, 2013, 60, 2493-2497.	1.6	60
5	Reliability Comparison of Triple-Gate Versus Planar SOI FETs. IEEE Transactions on Electron Devices, 2006, 53, 2351-2357.	1.6	47
6	Impact of silicidation on the excess noise behaviour of mos transistors. Solid-State Electronics, 1995, 38, 1893-1897.	0.8	46
7	Gate-all-around NWFETs vs. triple-gate FinFETs: Junctionless vs. extensionless and conventional junction devices with controlled EWF modulation for multi-VT CMOS. , 2015, , .		38
8	Low-Frequency Noise Performance of HfO[sub 2]-Based Gate Stacks. Journal of the Electrochemical Society, 2005, 152, F115.	1.3	36
9	Low-Frequency Noise Assessment of Silicon Passivated Ge pMOSFETs With TiN/TaN/ $hbox{HfO}_{2}$ Gate Stack. IEEE Electron Device Letters, 2007, 28, 288-291.	2.2	35
10	Tunneling 1/fÎ³ noise in 5nm HfO2/2.1nm SiO2 gate stack n-MOSFETs. Solid-State Electronics, 2005, 49, 702-707.	0.8	33
11	Impact of Forming Gas Annealing and Firing on the Al2O3/p-Si Interface State Spectrum. Electrochemical and Solid-State Letters, 2011, 14, H362.	2.2	30
12	Influence of the Source Composition on the Analog Performance Parameters of Vertical Nanowire-TFETs. IEEE Transactions on Electron Devices, 2015, 62, 16-22.	1.6	29
13	Study of line-TFET analog performance comparing with other TFET and MOSFET architectures. Solid-State Electronics, 2017, 128, 43-47.	0.8	29
14	Low-frequency noise assessment in advanced UTBOX SOI nMOSFETs with different gate dielectrics. Solid-State Electronics, 2014, 97, 14-22.	0.8	28
15	Calibration of Bulk Trap-Assisted Tunneling and Shockleyâ€“Readâ€“Hall Currents and Impact on InGaAs Tunnel-FETs. IEEE Transactions on Electron Devices, 2017, 64, 3622-3626.	1.6	28
16	Gate electrode effects on low-frequency (1/f) noise in p-MOSFETs with high-Îº dielectrics. Solid-State Electronics, 2006, 50, 992-998.	0.8	27
17	Low-Frequency Noise Investigation of GaN/AlGaN Metalâ€“Oxideâ€“Semiconductor High-Electron-Mobility Field-Effect Transistor With Different Gate Length and Orientation. IEEE Transactions on Electron Devices, 2020, 67, 3062-3068.	1.6	26
18	(Invited) Gate-All-Around Nanowire FETs vs. Triple-Gate FinFETs: On Gate Integrity and Device Characteristics. ECS Transactions, 2016, 72, 85-95.	0.3	25

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19	Junctionless Versus Inversion-Mode Gate-All-Around Nanowire Transistors From a Low-Frequency Noise Perspective. IEEE Transactions on Electron Devices, 2018, 65, 1487-1492.	1.6	25
20	A deep-level transient spectroscopy study of silicon interface states using different silicon nitride surface passivation schemes. Applied Physics Letters, 2010, 96, .	1.5	23
21	Defect profiling in FEFET Si:HfO2 layers. Applied Physics Letters, 2020, 117, .	1.5	23
22	Study of metal-related deep-level defects in germanide Schottky barriers on n-type germanium. Journal of Applied Physics, 2008, 104, .	1.1	22
23	Analytical Techniques for Electrically Active Defect Detection. Semiconductors and Semimetals, 2015, 91, 205-250.	0.4	22
24	DC and low frequency noise performances of SOI p-FinFETs at very low temperature. Solid-State Electronics, 2013, 90, 160-165.	0.8	21
25	Low frequency noise assessment in n- and p-channel sub-10nm triple-gate FinFETs: Part I: Theory and methodology. Solid-State Electronics, 2017, 128, 102-108.	0.8	21
26	The determination of deep level concentrations in high resistivity semiconductors by DLTS, with special reference to germanium. Journal Physics D: Applied Physics, 1985, 18, 2041-2058.	1.3	20
27	The temperature mobility degradation influence on the zero temperature coefficient of partially and fully depleted SOI MOSFETs. Microelectronics Journal, 2006, 37, 952-957.	1.1	20
28	Is there an impact of threading dislocations on the characteristics of devices fabricated in strainedâ€Ge substrates?. Physica Status Solidi C: Current Topics in Solid State Physics, 2009, 6, 1912-1917.	0.8	20
29	A DLTS Study of SiO2 and SiO2/SiNx Surface Passivation of Silicon. Journal of the Electrochemical Society, 2011, 158, H612.	1.3	20
30	Lowâ€“Frequency Noise in Vertically Stacked Si nâ€“Channel Nanosheet FETs. IEEE Electron Device Letters, 2020, 41, 317-320.	2.2	20
31	The 1/f/sup 1.7/ noise in submicron SOI MOSFETs with 2.5 nm nitrided gate oxide. IEEE Transactions on Electron Devices, 2002, 49, 2367-2370.	1.6	19
32	Impact of the Effective Work Function Gate Metal on the Low-Frequency Noise of Gate-All-Around Silicon-on-Insulator NWFETs. IEEE Electron Device Letters, 2016, 37, 363-365.	2.2	19
33	Low-Frequency-Noise Investigation of n-Channel Bulk FinFETs Developed for One-Transistor Memory Cells. IEEE Transactions on Electron Devices, 2012, 59, 1272-1278.	1.6	18
34	Defect engineering for shallow nâ€type junctions in germanium: Facts and fiction. Physica Status Solidi (A) Applications and Materials Science, 2016, 213, 2799-2808.	0.8	18
35	Reviewâ€”Device Assessment of Electrically Active Defects in High-Mobility Materials. ECS Journal of Solid State Science and Technology, 2016, 5, P3149-P3165.	0.9	18
36	Low-Frequency Noise Assessment of Vertically Stacked Si n-Channel Nanosheet FETs With Different Metal Gates. IEEE Transactions on Electron Devices, 2020, 67, 4802-4807.	1.6	18

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37	Analog Figures of Merit of Vertically Stacked Silicon Nanosheets nMOSFETs With Two Different Metal Gates for the Sub-7 nm Technology Node Operating at High Temperatures. IEEE Transactions on Electron Devices, 2021, 68, 3630-3635.	1.6	18
38	Electrically active defects at AlN/Si interface studied by DLTS and ESR. Physica Status Solidi (A) Applications and Materials Science, 2012, 209, 1851-1856.	0.8	17
39	Assessment of the Impact of Inelastic Tunneling on the Frequency-Depth Conversion from Low-Frequency Noise Spectra. IEEE Transactions on Electron Devices, 2014, 61, 634-637.	1.6	17
40	Low-Frequency Noise Characterization of GeO_{<italic>x</italic>} Passivated Germanium MOSFETs. IEEE Transactions on Electron Devices, 2015, 62, 2078-2083.	1.6	17
41	Diffusion and Gate Replacement: A New Gate-First High-<inline-formula> <tex-math notation="LaTeX">k </tex-math></inline-formula>/Metal Gate CMOS Integration Scheme Suppressing Gate Height Asymmetry. IEEE Transactions on Electron Devices, 2016, 63, 265-271.	1.6	16
42	Detailed characterisation of Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures. Solid-State Electronics, 2018, 143, 27-32.	0.8	16
43	Sidewall Crystalline Orientation Effect of Post-treatments for a Replacement Metal Gate Bulk Fin Field Effect Transistor. ACS Applied Materials & Interfaces, 2013, 5, 8865-8868.	4.0	15
44	Towards singleâ€trap spectroscopy: Generationâ€recombination noise in UTBOX SOI nMOSFETs. Physica Status Solidi C: Current Topics in Solid State Physics, 2015, 12, 292-298.	0.8	15
45	Probing the effect of point defects on the leakage blocking capability of Al0.1Ga0.9N/Si structures using a monoenergetic positron beam. Journal of Applied Physics, 2016, 120, .	1.1	15
46	Low frequency noise assessment in n- and p-channel sub-10nm triple-gate FinFETs: Part II: Measurements and results. Solid-State Electronics, 2017, 128, 109-114.	0.8	15
47	Detailed structural and electrical characterization of plated crystalline silicon solar cells. Solar Energy Materials and Solar Cells, 2018, 184, 57-66.	3.0	15
48	Dry Passivation Process for Silicon Heterojunction Solar Cells Using Hydrogen Plasma Treatment Followed by <italic>In Situ</italic> a-Si:H Deposition. IEEE Journal of Photovoltaics, 2018, 8, 1539-1545.	1.5	15
49	A deep-level analysis of Niâ€“Au/AlN/(1â€‰1â€‰1) p⁺-Si metalâ€“insulatorâ€“semiconductor capacitors. Journal Physics D: Applied Physics, 2011, 44, 475104.	1.3	14
50	Low-frequency noise assessment of border traps in Al₂O₃ capped DRAM peripheral MOSFETs. Semiconductor Science and Technology, 2014, 29, 115015.	1.0	14
51	Novel, Effective and Cost-Efficient Method of Introducing Fluorine into Metal/Hf-based Gate Stack in MuGFET and Planar SOI Devices with Significant BTI Improvement. , 2007, , .		13
52	Impact of the gate-electrode/dielectric interface on the low-frequency noise of thin gate oxide n-channel metal-oxide-semiconductor field-effect transistors. Solid-State Electronics, 2007, 51, 627-632.	0.8	13
53	Investigation of Preexisting and Generated Defects in Nonfilamentary a-Si/TiO₂ RRAM and Their Impacts on RTN Amplitude Distribution. IEEE Transactions on Electron Devices, 2018, 65, 970-977.	1.6	13
54	Effect of rotation, gate-dielectric and SEG on the noise behavior of advanced SOI MuGFETs. Solid-State Electronics, 2010, 54, 178-184.	0.8	12

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55	Low Frequency Noise Analysis for Post-Treatment of Replacement Metal Gate. IEEE Transactions on Electron Devices, 2013, 60, 2960-2962.	1.6	12
56	Low-Frequency Noise Assessment of Work Function Engineering Cap Layers in High-k Gate Stacks. ECS Journal of Solid State Science and Technology, 2019, 8, N25-N31.	0.9	12
57	Investigation of Light-Induced Deep-Level Defect Activation at the AlN/Si Interface. Applied Physics Express, 2011, 4, 094101.	1.1	11
58	Influence of 60-MeV Proton-Irradiation on Standard and Strained n- and p-Channel MuGFETs. IEEE Transactions on Nuclear Science, 2012, 59, 707-713.	1.2	11
59	Low-Frequency-Noise-Based Oxide Trap Profiling in Replacement High-Î²/Metal-Gate pMOSFETs. ECS Journal of Solid State Science and Technology, 2014, 3, Q127-Q131.	0.9	11
60	Low-Frequency Noise Assessment of the Oxide Trap Density in Thick-Oxide Input-Output Transistors for DRAM Applications. ECS Journal of Solid State Science and Technology, 2016, 5, N27-N31.	0.9	11
61	Understanding Frequency Dependence of Trap Generation Under AC Negative Bias Temperature Instability Stress in Si p-FinFETs. IEEE Electron Device Letters, 2020, 41, 965-968.	2.2	11
62	Analog design with Line-TFET device experimental data: from device to circuit level. Semiconductor Science and Technology, 2020, 35, 055025.	1.0	11
63	Deep-level transient spectroscopy of Al/a-Si:H/c-Si structures for heterojunction solar cell applications. Journal of Applied Physics, 2014, 116, .	1.1	10
64	Border Traps in InGaAs nMOSFETs Assessed by Low-Frequency Noise. IEEE Electron Device Letters, 2014, 35, 720-722.	2.2	10
65	Analysis of Leakage Mechanisms in AlN Nucleation Layers on p-Si and p-SOI Substrates. IEEE Transactions on Electron Devices, 2019, 66, 1849-1855.	1.6	10
66	Low-Frequency Noise Characterization of Germanium n-Channel FinFETs. IEEE Transactions on Electron Devices, 2020, 67, 2872-2877.	1.6	10
67	(Invited) Replacement Metal Gate/High-k Last Technology for Aggressively Scaled Planar and FinFET-Based Devices. ECS Transactions, 2014, 61, 225-235.	0.3	9
68	GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes. IEEE Electron Device Letters, 2016, 37, 1092-1095.	2.2	9
69	Electrical Effects of a Single Extended Defect in MOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 3069-3075.	1.6	9
70	Investigation of Defect Characteristics and Carrier Transport Mechanisms in GaN Layers With Different Carbon Doping Concentration. IEEE Transactions on Electron Devices, 2020, 67, 4827-4833.	1.6	9
71	Impact of Dummy Gate Removal and a Silicon Cap on the Low-Frequency Noise Performance of Germanium nFinFETs. IEEE Transactions on Electron Devices, 2020, 67, 4713-4719.	1.6	9
72	Overview of Bias Temperature Instability in Scaled DRAM Logic for Memory Transistors. IEEE Transactions on Device and Materials Reliability, 2020, 20, 258-268.	1.5	9

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73	Low frequency noise performance of horizontal, stacked and vertical silicon nanowire MOSFETs. Solid-State Electronics, 2021, 184, 108087.	0.8	9
74	Characterization of Oxide Precipitates in Heavily B-Doped Silicon by Infrared Spectroscopy. Journal of the Electrochemical Society, 2004, 151, G598.	1.3	8
75	A new high-k/metal gate CMOS integration scheme (Diffusion and Gate Replacement) suppressing gate height asymmetry and compatible with high-thermal budget memory technologies. , 2014, , .		8
76	Low-Frequency Noise Assessment of Different Ge pFinFET STI Processes. IEEE Transactions on Electron Devices, 2016, 63, 4031-4037.	1.6	8
77	Treatments for reliability improvement in thick oxides diffusion and gate replacement I/O transistors. International Journal of Materials Engineering Innovation, 2017, 8, 53.	0.2	8
78	Low Frequency Noise Analysis of Impact of Metal Gate Processing on the Gate Oxide Stack Quality. ECS Journal of Solid State Science and Technology, 2018, 7, Q26-Q32.	0.9	8
79	Physical Mechanism Underlying the Time Exponent Shift in the Ultra-fast NBTI of High-k/Metal gated p-CMOSFETs. , 2018, , .		8
80	TaN Versus TiN Metal Gate Input/Output pMOSFETs: A Low-Frequency Noise Perspective. IEEE Transactions on Electron Devices, 2018, 65, 3676-3681.	1.6	8
81	Zero-Temperature-Coefficient of planar and MuGFET SOI devices. , 2010, , .		7
82	Direct estimation of capture cross sections in the presence of slow capture: application to the identification of quenched-in deep-level defects in Ge. Semiconductor Science and Technology, 2014, 29, 125007.	1.0	7
83	Comparative analysis of the intrinsic voltage gain and unit gain frequency between SOI and bulk FinFETs up to high temperatures. Solid-State Electronics, 2016, 123, 124-129.	0.8	7
84	Gate Metal and Cap Layer Effects on Ge nMOSFETs Low-Frequency Noise Behavior. IEEE Transactions on Electron Devices, 2019, 66, 1050-1056.	1.6	7
85	Impact of ALD TiN Capping Layer on Interface Trap and Channel Hot Carrier Reliability of HKMG nMOSFETs. IEEE Electron Device Letters, 2018, 39, 1129-1132.	2.2	6
86	Using the Octagonal Layout Style for MOSFETs to Boost the Device Matching in Ionizing Radiation Environments. IEEE Transactions on Device and Materials Reliability, 2020, 20, 754-759.	1.5	6
87	Deep-level transient spectroscopy of detector-grade high-resistivity float-zone silicon. Journal of Electronic Materials, 1992, 21, 533-541.	1.0	5
88	Low-frequency noise measurements at liquid helium temperature operation in ultra-thin buried oxide transistors â€“ Physical interpretation of transport phenomena. Solid-State Electronics, 2018, 150, 1-7.	0.8	5
89	Dry etch damage in n-type crystalline silicon wafers assessed by deep-level transient spectroscopy and minority carrier lifetime. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2018, 36, 041201.	0.6	5
90	Reliability Engineering Enabling Continued Logic for Memory Device Scaling. , 2019, , .		5

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91	Deep-Level Transient Spectroscopy of <mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" overflow="scroll"><mml:mrow><mml:mi>Ga</mml:mi><mml:mi>As</mml:mi></mml:mrow></mml:math> Nanoridge Diodes Grown on <mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" overflow="scroll"><mml:mi>Si</mml:mi></mml:math> Substrates. Physical Review Applied, 2020, 14, .	1.5	5
92	Comparative study on NBTI kinetics in Si p-FinFETs with B2H6-based and SiH4-based atomic layer deposition tungsten (ALD W) filling metal. Microelectronics Reliability, 2020, 107, 113627.	0.9	5
93	Low-frequency noise of n-type triple gate FinFETs fabricated on standard and 45Â° rotated substrates. Solid-State Electronics, 2013, 90, 121-126.	0.8	4
94	Impact of Al<inf>2</inf>O<inf>3</inf> position on performances and reliability in high-k metal gated DRAM periphery transistors. , 2013, , .		4
95	Effective hole mobility and low-frequency noise characterization of Ge pFinFETs. , 2016, , .		4
96	On trap identification in triple-gate FinFETs and Gate-All-Around nanowire MOSFETs using low frequency noise spectroscopy. , 2017, , .		4
97	Defect Characterization in Highâ€Electronâ€Mobility Transistors with Regrown pâ€GaN Gate by Lowâ€Frequency Noise and Deepâ€Level Transient Spectroscopy. Physica Status Solidi (A) Applications and Materials Science, 0, , 2100227.	0.8	4
98	Low-Frequency noise investigation of AlGaN/GaN high-electron-mobility transistors. Solid-State Electronics, 2021, 183, 108050.	0.8	4
99	Low-frequency noise assessment of ferro-electric field-effect transistors with Si-doped HfO2 gate dielectric. AIP Advances, 2021, 11, .	0.6	4
100	Low-frequency noise analysis of DRAM peripheral transistors with La cap. , 2014, , .		3
101	Proton Radiation Effects on the Analog Performance of Bulk n- and p-FinFETs. ECS Transactions, 2015, 66, 295-301.	0.3	3
102	Different stress techniques and their efficiency on triple-gate SOI n-MOSFETs. Solid-State Electronics, 2015, 103, 209-215.	0.8	3
103	Insights into the reliability of Ni/Cu plated p-PERC silicon solar cells. Energy Procedia, 2017, 124, 862-868.	1.8	3
104	The Influence of Oxide Thickness and Indium Amount on the Analog Parameters of In_{<italic>x</italic>}Ga_{1â€“<italic>x</italic>}As nTFETs. IEEE Transactions on Electron Devices, 2017, 64, 3595-3600.	1.6	3
105	Impact of the silicon substrate resistivity and growth condition on the deep levels in Ni-Au/AlN/Si MIS Capacitors. Semiconductor Science and Technology, 2017, 32, 105002.	1.0	3
106	Impact of In Situ Annealing on the Deep Levels in Niâ€Au/AlN/Si Metalâ€“Insulatorâ€“Semiconductor Capacitors. Physica Status Solidi (A) Applications and Materials Science, 2019, 216, 1900248.	0.8	3
107	Intrinsic Voltage Gain of Stacked GAA Nanosheet MOSFETs Operating at High Temperatures. ECS Transactions, 2020, 97, 65-69.	0.3	3
108	Insights Into the Effect of TiN Thickness Scaling on DC and AC NBTI Characteristics in Replacement Metal Gate pMOSFETs. IEEE Transactions on Device and Materials Reliability, 2020, 20, 498-505.	1.5	3

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109	An Investigation of Field Reduction Effect on NBTI Parameter Characterization and Lifetime Prediction Using a Constant Field Stress Method. IEEE Transactions on Device and Materials Reliability, 2020, 20, 92-96.	1.5	3
110	Low temperature investigation of n-channel GAA vertically stacked silicon nanosheets. , 2021, , .		3
111	Impact of thermal budget on the low-frequency noise of DRAM peripheral nMOSFETs. , 2015, , .		2
112	Deep level investigation of INGAAS on INP layer. , 2017, , .		2
113	Comparison between proton irradiated triple gate SOI TFETS and finfets from a TID point of view. Semiconductor Science and Technology, 2019, 34, 065003.	1.0	2
114	Impact of Device Architecture and Gate Stack Processing on the Low-Frequency Noise of Silicon Nanowire Transistors. , 2019, , .		2
115	Improved physics-based analysis to discriminate the flicker noise origin at very low temperature and drain voltage polarization. Solid-State Electronics, 2020, 171, 107771.	0.8	2
116	Electrical Activity of Extended Defects in Relaxed In_xGa_{1â^'x}As Hetero-Epitaxial Layers. ECS Journal of Solid State Science and Technology, 2020, 9, 033001.	0.9	2
117	Interfacial Properties of nMOSFETs With Different Al2O3 Capping Layer Thickness and TiN Gate Stacks. IEEE Transactions on Electron Devices, 2021, 68, 948-953.	1.6	2
118	Horizontal, Stacked or Vertical Silicon Nanowires: Does it Matter from a Low-Frequency Noise Perspective?. , 2020, , .		2
119	Parasitic subthreshold drain current and low frequency noise in GaN/AlGaN metal-oxide-semiconductor high-electron-mobility field-effect-transistors. Semiconductor Science and Technology, 2021, 36, 024003.	1.0	2
120	On the asymmetry of the DC and low-frequency noise characteristics of vertical nanowire MOSFETs with bulk source contact. Solid-State Electronics, 2022, 191, 108268.	0.8	2
121	Temperature-Dependent Electrical Properties of nMOSFETs With Different Thickness Alâ„Oâ„ƒ Capping Layer and TiN Gate. IEEE Transactions on Electron Devices, 2021, 68, 6020-6025.	1.6	2
122	DC and low a frequency noise analysis of p channel gate all around vertically stacked silicon nanosheets. Solid-State Electronics, 2022, 194, 108360.	0.8	2
123	Linking Room- and Low-Temperature Electrical Performance of MOS Gate Stacks for Cryogenic Applications. IEEE Electron Device Letters, 2022, 43, 674-677.	2.2	2
124	Comparison between Si/SiO₂ midâ€gap interface states and deep levels associated with siliconâ€oxygen superlattices in pâ€type silicon. Physica Status Solidi C: Current Topics in Solid State Physics, 2016, 13, 718-723.	0.8	1
125	Comparative Study of Current Transients in HPHT and CVD Diamond Capacitor-Sensors. ECS Journal of Solid State Science and Technology, 2016, 5, P3101-P3107.	0.9	1
126	Low frequency noise and fin width study of silicon passivated germanium pFinFETs. , 2016, , .		1

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127	Deep Level Assessment of n-Type Si/SiO₂Metal-Oxide-Semiconductor Capacitors with Embedded Ge Quantum Dots. ECS Journal of Solid State Science and Technology, 2018, 7, P24-P28.	0.9	1
128	Impact of band to band tunneling in In0.53Ga0.47As tunnel diodes on the deep level transient spectra. Applied Physics Letters, 2018, 113, 232101.	1.5	1
129	Do we have to worry about extended defects in high-mobility materials?. , 2018, , .		1
130	Deep levels in metalâ€“oxideâ€“semiconductor capacitors fabricated on n-type In0.53Ga0.47As lattice matched to InP substrates. Semiconductor Science and Technology, 2019, 34, 075024.	1.0	1
131	A DLTS Perspective on Electrically Active Defects in Plated Crystalline Silicon n⁺p Solar Cells. ECS Journal of Solid State Science and Technology, 2019, 8, P693-P698.	0.9	1
132	Alleviation of negative-bias temperature instability in Si p-FinFETs with ALD W Gate-Filling Metal by Annealing Process optimization. IEEE Journal of the Electron Devices Society, 2021, , 1-1.	1.2	1
133	Current mirror designed with GAA nanosheet MOSFETs from room temperature to 200 Â°C. Semiconductor Science and Technology, 2021, 36, 095019.	1.0	1
134	Recovery Behavior of Interface Traps After Negative Bias Temperature Instability Stress in p-FinFETs Featuring Fast Trap Characterization Technique. IEEE Transactions on Electron Devices, 2021, 68, 4251-4258.	1.6	1
135	Characterization of defect states in Mg-doped GaN-on-Si p+n diodes using deep-level transient Fourier spectroscopy. Semiconductor Science and Technology, 2020, 36, 024002.	1.0	1
136	Analysis of semi-insulating carbon-doped GaN layers using deep-level transient spectroscopy. Journal of Applied Physics, 2021, 130, 205701.	1.1	1
137	Design of operational transconductance amplifier with Gate-All-Around Nanosheet MOSFET using experimental data from room temperature to 200ÂÂ°C. Solid-State Electronics, 2022, 189, 108238.	0.8	1
138	Lifetime assessment of In _x Ga _{1â€x} As nâ€type heteroâ€epitaxial layers. Physica Status Solidi (A) Applications and Materials Science, 0, , .	0.8	1
139	Can we optimize the gate oxide quality of DRAM input/output pMOSFETs by a post-deposition treatment?. Semiconductor Science and Technology, 2019, 34, 015017.	1.0	0
140	A Deep Level Transient Spectroscopy Study of Hole Traps in GexSe1â^'x-based Layers for Ovonic Threshold Switching Selectors. ECS Journal of Solid State Science and Technology, 2020, 9, 044006.	0.9	0
141	Frontiers in Low-Frequency Noise Research in Advanced Semiconductor Devices. , 2021, , .		0
142	A Fast DCIV Technique for Characterizing the Generation and Repassivation of Interface Traps Under DC/ AC NBTI Stress/Recovery Condition in Si p-FinFETs. , 2021, , .		0
143	Low Frequency Noise: A Show Stopper for State-of-the-art and Future Si, Ge-based and III-V Technologies. , 2021, , .		0
144	Analysis of the ZTC-Point for Vertically Stacked Nanosheet pMOS Devices. , 2021, , .		0

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145	High Temperature Influence on the Trade-off between gm/I_D and f_T of nanosheet NMOS Transistors with Different Metal Gate Stack. , 2021, , .		0
146	Experimental Analysis of Trade-Off Between Transistor Efficiency and Unit Gain Frequency of Nanosheet NMOS Transistors. , 2021, , .		0
147	Comparison of DC/AC Hot Carrier Degradation between Short Channel Si Bulk and SiGe SOI p-FinFETs. , 2021, , .		0
148	Trade-off analysis between gm/ID and fT of nanosheet NMOS transistors with different metal gate stack at high temperature. Solid-State Electronics, 2022, 191, 108267.	0.8	0
149	Impact of the Channel Doping on the Low-Frequency Noise of Silicon Vertical Nanowire pFETs. Solid-State Electronics, 2022, , 108318.	0.8	0
150	Study of Electron Traps Associated With Oxygen Superlattices in nâ€Type Silicon. Physica Status Solidi C: Current Topics in Solid State Physics, 2017, 14, 1700136.	0.8	0