Huan-Lin Chang

List of Publications by Year
in descending order

26	451	1040056 9	1125743 13
papers	citations	h-index	g-index

26	26	26	514
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Core Model for Independent Multigate MOSFETs. , 2019, , 15-34.		0
2	BSIM-HV: High-Voltage MOSFET Model Including Quasi-Saturation and Self-Heating Effect. IEEE Transactions on Electron Devices, 2019, 66, 4258-4263.	3.0	23
3	Designing 0.5 V 5-nm HP and 0.23 V 5-nm LP NC-FinFETs With Improved ${I}_{ mathrm{scriptscriptstyle OFF}}$ Sensitivity in Presence of Parasitic Capacitance. IEEE Transactions on Electron Devices, 2018, 65, 1211-1216.	3.0	31
4	Engineering Negative Differential Resistance in NCFETs for Analog Applications. IEEE Transactions on Electron Devices, 2018, 65, 2033-2039.	3.0	79
5	New Mobility Model for Accurate Modeling of Transconductance in FDSOI MOSFETs. IEEE Transactions on Electron Devices, 2018, 65, 463-469.	3.0	5
6	Modeling of Advanced RF Bulk FinFETs. IEEE Electron Device Letters, 2018, 39, 791-794.	3.9	17
7	Effect of Polycrystallinity and Presence of Dielectric Phases on NC-FinFET Variability. , 2018, , .		14
8	Negative-Capacitance FinFETs: Numerical Simulation, Compact Modeling and Circuit Evaluation. , 2018, , .		9
9	Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor. IEEE Transactions on Electron Devices, 2018, 65, 4652-4658.	3.0	29
10	A Predictive Tunnel FET Compact Model With Atomistic Simulation Validation. IEEE Transactions on Electron Devices, 2017, 64, 599-605.	3.0	20
11	Compact Modeling Source-to-Drain Tunneling in Sub-10-nm GAA FinFET With Industry Standard Model. IEEE Transactions on Electron Devices, 2017, 64, 3576-3581.	3.0	13
12	Modeling of Back-Gate Effects on Gate-Induced Drain Leakage and Gate Currents in UTB SOI MOSFETs. IEEE Transactions on Electron Devices, 2017, 64, 3986-3990.	3.0	9
13	Modeling of GeOI and validation with Ge-CMOS inverter circuit using BSIM-IMG industry standard model. , 2016, , .		6
14	Predictive effective mobility model for FDSOI transistors using technology parameters. , 2016, , .		6
15	Compact models of negative-capacitance FinFETs: Lumped and distributed charge models. , 2016, , .		69
16	Modeling of Subsurface Leakage Current in Low Short Channel MOSFET at Accumulation Bias. IEEE Transactions on Electron Devices, 2016, 63, 1840-1845.	3.0	14
17	Modeling of threshold voltage for operating point using industry standard BSIM-IMG model. , 2016, , .		6
18	Physical mechanism of HfO<inf>2</inf>-based bipolar resistive random access memory. , 2011, , .		11

#	Article	IF	Citations
19	A parameterized SPICE macromodel of resistive random access memory and circuit demonstration. , 2011, , .		3
20	Voltage Linearity Improvement of HfO[sub 2]-Based Metalâ€“Insulatorâ€“Metal Capacitors with H[sub 2]O Prepulse Treatment. Journal of the Electrochemical Society, 2011, 158, H128.	2.9	3
21	Improved SPICE macromodel of phase change random access memory. , 2009, , .		6
22	Stress-Induced Hump Effects of p-Channel Polycrystalline Silicon Thin-Film Transistors. IEEE Electron Device Letters, 2008, 29, 1332-1335.	3.9	66
23	Reduction of Crosstalk Between Dual Power Amplifiers Using Laser Treatment. IEEE Microwave and Wireless Components Letters, 2008, 18, 602-604.	3.2	0
24	Performance Enhancement of the nMOSFET Low-Noise Amplifier by Package Strain. IEEE Transactions on Electron Devices, 2007, 54, 160-162.	3.0	1
25	Differential power combining technique for general power amplifiers using lumped component network. , 2006, , .		0
26	Coupling Effects of Dual SiGe Power Amplifiers for 802.11n MIMO Applications. , 0, , .		11