Andrzej Mazurak

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	Technology and characterization of MIS structures with co-doped silicon nanocrystals (Si-NCs) embedded in hafnium oxide (HfOx) ultra-thin layers. Microelectronic Engineering, 2017, 178, 298-303.	2.4	9
2	Silicon-Carbide (SiC) Nanocrystal Technology and Characterization and Its Applications in Memory Structures. Nanomaterials, 2020, 10, 2387.	4.1	8
3	Investigation of Electrical Properties of the Al/SiO2/n++-Si Resistive Switching Structures by Means of Static, Admittance, and Impedance Spectroscopy Measurements. Materials, 2021, 14, 6042.	2.9	8
4	Small-signal admittance model of multi-traps distributed over energy and space in the insulator of MIS tunnel structures. Microelectronic Engineering, 2015, 147, 349-353.	2.4	6
5	Some Issues of Modeling the Double Barrier Metal-Oxide-Semiconductor Tunnel Structures. Advanced Materials Research, 2011, 276, 77-85.	0.3	4
6	Effect of nanocrystal geometric location on tunnel currents and smallâ€signal admittance of MIS structures. Physica Status Solidi C: Current Topics in Solid State Physics, 2016, 13, 1035-1039.	0.8	3
7	Study of the effect of tunneling through the traps inside the insulator on small-signal admittance of the MOS structure. Microelectronic Engineering, 2013, 109, 1-4.	2.4	2
8	Simulations of transient processes and characteristics of the nc-MOS structures. Microelectronic Engineering, 2017, 178, 173-177.	2.4	2
9	Stressâ€andâ€5ense Investigation of Memory Effect in Siâ€NCs MIS Structures. Physica Status Solidi (B): Basic Research, 2018, 255, 1700634.	1.5	2
10	Determination of border/bulk traps parameters based on (<i>C</i> - <i>G</i> - <i>V</i>) admittance measurements. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2019, 37, .	1.2	2
11	Comparison of memory effect with voltage or current charging pulse bias in MIS structures based on codoped Si-NCs embedded in SiO2 or HfOx. Solid-State Electronics, 2019, 159, 157-164.	1.4	2
12	WKB approximation based formula for tunneling probability through a multi-layer potential barrier. , 2012, , .		1
13	Frequency Modulated C-V Characteristics Shift in Double-layer High-k Gate Stack MIS Devices. , 2020, , .		1
14	Investigation of current-voltage characteristics of the transistor structures with double-potential barrier DBMOS. , 2013, , .		0
15	Investigation of temperature effect on electrical characteristics of the double barrier metal-oxide-semiconductor structure. , 2013, , .		0
16	Effect of interface traps parameters on admittance characteristics of the MIS (metal-insulator-semiconductor) tunnel structures. Proceedings of SPIE, 2016, , .	0.8	0
17	Investigation of memory effect with voltage or current charging pulse bias in MIS structures based on codoped Si-NCs. , 2018, , .		0
18	Memory effect in MIS structures with embedded all-inorganic colloidal silicon carbide (SiC) nanocrystals. , 2019, , .		0

#	Article	IF	CITATIONS
19	Investigation of the anomalous effect of the AC-signal frequency on flat-band voltage of Al/HfO2/SiO2/Si structures. Solid-State Electronics, 2021, 183, 108107.	1.4	0