

# YunSeop Yu

## List of Publications by Year in descending order

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citations

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91  
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docs citations

91  
times ranked

612  
citing authors

#	ARTICLE	IF	CITATIONS
1	Macromodeling of single-electron transistors for efficient circuit simulation. IEEE Transactions on Electron Devices, 1999, 46, 1667-1671.	3.0	72
2	Fall-Detection Algorithm Using 3-Axis Acceleration: Combination with Simple Threshold and Hidden Markov Model. Journal of Applied Mathematics, 2014, 2014, 1-8.	0.9	57
3	Design challenges and solutions for ultra-high-density monolithic 3D ICs. , 2014, , .		39
4	Analytical Threshold Voltage Model Including Effective Conducting Path Effect (ECPE) for Surrounding-Gate MOSFETs (SGMOSFETs) With Localized Charges. IEEE Transactions on Electron Devices, 2010, 57, 3176-3180.	3.0	29
5	Single-Electron-Based Flexible Multivalued Exclusive-or Logic Gate. IEEE Transactions on Electron Devices, 2009, 56, 1048-1055.	3.0	26
6	A Unified Analytical Current Model for N- and P-Type Accumulation-Mode (Junctionless) Surrounding-Gate Nanowire FETs. IEEE Transactions on Electron Devices, 2014, 61, 3007-3010.	3.0	26
7	Impact of Quantum Confinement on Band-to-Band Tunneling of Line-Tunneling Type L-Shaped Tunnel Field-Effect Transistor. IEEE Transactions on Electron Devices, 2019, 66, 2010-2016.	3.0	26
8	Subthreshold Degradation of Gate-all-Around Silicon Nanowire Field-Effect Transistors: Effect of Interface Trap Charge. IEEE Electron Device Letters, 2011, 32, 1179-1181.	3.9	20
9	One electron-based smallest flexible logic cell. Applied Physics Letters, 2012, 101, .	3.3	18
10	Electrical Coupling of Monolithic 3-D Inverters. IEEE Transactions on Electron Devices, 2016, , 1-4.	3.0	18
11	Interface Trap Density of Gate-All-Around Silicon Nanowire Field-Effect Transistors With TiN Gate: Extraction and Compact Model. IEEE Transactions on Electron Devices, 2013, 60, 2457-2463.	3.0	18
12	Transient modelling of single-electron transistors for efficient circuit simulation by SPICE. IET Circuits, Devices and Systems, 2005, 152, 691.	0.6	17
13	All-analytic surface potential model for SOI MOSFETs. IET Circuits, Devices and Systems, 2005, 152, 183.	0.6	17
14	Equivalent Circuit Model of Semiconductor Nanowire Diode by SPICE. Journal of Nanoscience and Nanotechnology, 2007, 7, 4089-4093.	0.9	16
15	A SPICE-Compatible New Silicon Nanowire Field-Effect Transistors (SNWFETs) Model. IEEE Nanotechnology Magazine, 2009, 8, 643-649.	2.0	16
16	Physical Parameter-Based SPICE Models for InGaZnO Thin-Film Transistors Applicable to Process Optimization and Robust Circuit Design. IEEE Electron Device Letters, 2012, 33, 59-61.	3.9	15
17	Implicit Continuous Current-Voltage Model for Surrounding-Gate Metal-Oxide-Semiconductor Field-Effect Transistors Including Interface Traps. IEEE Transactions on Electron Devices, 2011, 58, 2520-2524.	3.0	13
18	Barrier Height at the Graphene and Carbon Nanotube Junction. IEEE Transactions on Electron Devices, 2014, 61, 2203-2207.	3.0	13

#	ARTICLE	IF	CITATIONS
19	Equivalent circuit approach for single electron transistor model for efficient circuit simulation by SPICE. Electronics Letters, 2002, 38, 850.	1.0	12
20	Double-dot-like charge transport through a small size silicon single electron transistor. Physica E: Low-Dimensional Systems and Nanostructures, 2002, 13, 946-949.	2.7	11
21	Two-dimensional (2D) transition metal dichalcogenide semiconductor field-effect transistors: the interface trap density extraction and compact model. Semiconductor Science and Technology, 2015, 30, 075010.	2.0	11
22	A Physics-Based, SPICE (Simulation Program with Integrated Circuit Emphasis)-Compatible Non-Quasi-Static MOS (Metal-Oxide-Semiconductor) Transient Model Based on the Collocation Method. Japanese Journal of Applied Physics, 1998, 37, L119-L121.	1.5	10
23	Electrical Characteristics of the Backgated Bottom-Up Silicon Nanowire FETs. IEEE Nanotechnology Magazine, 2008, 7, 683-687.	2.0	10
24	Full-Range Analytic Drain Current Model for Depletion-Mode Long-Channel Surrounding-Gate Nanowire Field-Effect Transistor. Journal of Semiconductor Technology and Science, 2013, 13, 361-366.	0.4	10
25	Green-function approach to transport through a gate-surrounded Si nanowire with impurity scattering. Physical Review B, 2008, 77, .	3.2	9
26	Microwave Characterization of a Field Effect Transistor with Dielectrophoretically-Aligned Single Silicon Nanowire. Japanese Journal of Applied Physics, 2010, 49, 06GG12.	1.5	9
27	Axial $\pi$ Nanowire Gated Diodes as a Direct Probe of Surface-Dominated Charge Dynamics in Semiconductor Nanomaterials. Journal of Physical Chemistry C, 2011, 115, 23552-23557.	3.1	9
28	Gate All Around Metal Oxide Field Transistor: Surface Potential Calculation Method including Doping and Interface Trap Charge and the Effect of Interface Trap Charge on Subthreshold Slope. Journal of Semiconductor Technology and Science, 2013, 13, 530-537.	0.4	9
29	Work-Function Engineering of Source-Overlapped Dual-Gate Tunnel Field-Effect Transistor. Journal of Nanoscience and Nanotechnology, 2018, 18, 5925-5931.	0.9	8
30	Investigation of Monolithic 3D Integrated Circuit Inverter with Feedback Field Effect Transistors Using TCAD Simulation. Micromachines, 2020, 11, 852.	2.9	8
31	Electrical Coupling and Simulation of Monolithic 3D Logic Circuits and Static Random Access Memory. Micromachines, 2019, 10, 637.	2.9	7
32	Compact Trap-Assisted-Tunneling Model for Line Tunneling Field-Effect-Transistor Devices. Applied Sciences (Switzerland), 2020, 10, 4475.	2.5	7
33	Metal oxide-graphene field-effect transistor: interface trap density extraction model. Beilstein Journal of Nanotechnology, 2016, 7, 1368-1376.	2.8	6
34	Temperature-Dependent Electrical Characterization of Amorphous Indium Zinc Oxide Thin-Film Transistors. IEEE Transactions on Electron Devices, 2017, 64, 3183-3188.	3.0	6
35	Compact Model for L-Shaped Tunnel Field-Effect Transistor Including the 2D Region. Applied Sciences (Switzerland), 2019, 9, 3716.	2.5	6
36	Parameter Extraction and Power/Performance Analysis of Monolithic 3-D Inverter (M3INV). IEEE Transactions on Electron Devices, 2019, 66, 1006-1011.	3.0	6

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37	Multi-valued static random access memory (SRAM) cell with single-electron and MOSFET hybrid circuit. <i>Electronics Letters</i> , 2005, 41, 1316.	1.0	5
38	Gate bias controlled NDR in an in-plane-gate quantum dot transistor. <i>Physica E: Low-Dimensional Systems and Nanostructures</i> , 2006, 32, 532-535.	2.7	5
39	A compact analytical current conduction model for a depletion-mode n-type nanowire field-effect transistor with a bottom-gate structure. <i>Semiconductor Science and Technology</i> , 2008, 23, 035025.	2.0	5
40	Fabrication and Characterization of Sidewall Defined Silicon-on-Insulator Single-Electron Transistor. <i>IEEE Nanotechnology Magazine</i> , 2008, 7, 544-550.	2.0	5
41	Optimization of Line-Tunneling Type L-Shaped Tunnel Field-Effect-Transistor for Steep Subthreshold Slope. <i>Electronics (Switzerland)</i> , 2018, 7, 275.	3.1	5
42	Fall Recognition Algorithm Using Gravity-Weighted 3-Axis Accelerometer Data. <i>Journal of the Institute of Electronics and Information Engineers</i> , 2013, 50, 254-259.	0.0	5
43	Fabrication and characterization of metal-semiconductor field-effect-transistor-type quantum devices. <i>Journal of Applied Physics</i> , 2004, 96, 704-708.	2.5	4
44	Compact device modelling of interface trap charges with quantum capacitance in MoS <sub>2</sub> -based field-effect transistors. <i>Semiconductor Science and Technology</i> , 2020, 35, 045023.	2.0	4
45	Modeling of Semiconductor Nanowire Field-Effect Transistors Considering Schottky-Barrier-Height Lowering. <i>Journal of the Korean Physical Society</i> , 2007, 51, 298.	0.7	4
46	A half-adder (HA) and a full-adder (FA) combining single-electron transistors (SETs) with MOSFETs. <i>Semiconductor Science and Technology</i> , 2007, 22, 647-652.	2.0	3
47	Observation of gate bias dependent interface coupling in thin silicon-on-insulator metal-oxide-semiconductor field-effect transistors. <i>Journal of Applied Physics</i> , 2007, 102, 034509.	2.5	3
48	Hybrid integration of GaAs/AlGaAs in-plane-gate resonant tunneling and field effect transistors. <i>Physica E: Low-Dimensional Systems and Nanostructures</i> , 2008, 40, 2160-2162.	2.7	3
49	A power-, delay- and emergency-efficient protocol of ubiquitous sensor network systems for silver town applications. <i>Journal of Supercomputing</i> , 2010, 54, 122-137.	3.6	3
50	Single-String Carbon Nanotube Field Effect Transistors Fabricated by Two-Step Dielectrophoresis. <i>Japanese Journal of Applied Physics</i> , 2012, 51, 06FE02.	1.5	3
51	Investigation of Corner Effect and Identification of Tunneling Regimes in L-Shaped Tunnel Field-Effect-Transistor. <i>Journal of Nanoscience and Nanotechnology</i> , 2018, 18, 6575-6583.	0.9	3
52	Transmission-Type Radio-Frequency Single-Electron Transistor with In-Plane-Gate Single-Electron Transistor. <i>Japanese Journal of Applied Physics</i> , 2007, 46, 2592-2595.	1.5	2
53	Fabrication and Characterization of a Double Quantum Dot Structure. <i>Journal of Nanoscience and Nanotechnology</i> , 2008, 8, 5009-5013.	0.9	2
54	Explicit Continuous Current-Voltage ( $I-V$ ) Models for Fully-Depleted Surrounding-Gate MOSFETs (SGMOSFETs) with a Finite Doping Body. <i>Journal of Nanoscience and Nanotechnology</i> , 2010, 10, 3316-3320.	0.9	2

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55	Analytic Model of a Silicon Nanowire pH Sensor. Journal of Nanoscience and Nanotechnology, 2011, 11, 10809-10812.	0.9	2
56	Coupling capacitance in face-to-face (F2F) bonded 3D ICs: Trends and implications. , 2015, , .		2
57	Electrical Characteristics of Ge/Si-Based Source Pocket Tunnel Field-Effect Transistors. Journal of Nanoscience and Nanotechnology, 2018, 18, 5887-5892.	0.9	2
58	Si/Ge Hetero Tunnel Field-Effect Transistor with Junctionless Channel Based on Nanowire. Journal of Nanoscience and Nanotechnology, 2019, 19, 6750-6754.	0.9	2
59	Physically Consistent Method for Calculating Trap-Assisted-Tunneling Current Applied to Line Tunneling Field-Effect Transistor. IEEE Transactions on Electron Devices, 2020, 67, 2106-2112.	3.0	2
60	Macro-Modeling for N-Type Feedback Field-Effect Transistor for Circuit Simulation. Micromachines, 2021, 12, 1174.	2.9	2
61	Compact Model of a pH Sensor with Depletion-Mode Silicon-Nanowire Field-Effect Transistor. Journal of Semiconductor Technology and Science, 2014, 14, 451-456.	0.4	2
62	Simulation method of transmission-type Radio-Frequency Single-Electron Transistor (RF-SET) by SPICE. , 2006, , .		1
63	Design of A Power-, Delay-, and Emergency-Efficient Protocol of Ubiquitous Sensor Network Systems for Silver Town Applications. , 2008, , .		1
64	Continuous analytic current-voltage (I <sub>D</sub> -V) model for long-channel doped surrounding-gate MOSFETs (SGMOSFETs). , 2008, , .		1
65	Radio frequency electrical pulse characterization of defect states in a GaAs/AlGaAs narrow channel field effect transistor. Semiconductor Science and Technology, 2009, 24, 085018.	2.0	1
66	Fabrication and Characterization of an Enhancement-Mode Planar Resonant Tunneling Transistor. IEEE Nanotechnology Magazine, 2010, 9, 123-127.	2.0	1
67	Analytic Modeling of a Depletion-Mode Cylindrical Surrounding-Gate Nanowire Field-Effect Transistor. Journal of Nanoscience and Nanotechnology, 2012, 12, 5925-5929.	0.9	1
68	One electron-controlled multiple-valued dynamic random-access-memory. AIP Advances, 2016, 6, 025320.	1.3	1
69	Improvements in adhesion force and smart embedded programming of wall inspection robot. Journal of Supercomputing, 2016, 72, 2635-2650.	3.6	1
70	Circuit Simulation Considering Electrical Coupling in Monolithic 3D Logics with Junctionless FETs. Micromachines, 2020, 11, 887.	2.9	1
71	Comparison of Two-Types of Monolithic 3D Inverter Consisting of MOSFETs and Junctionless FETs. , 2020, , .		1
72	Interface trap density distribution in 3D sequential Integrated-Circuit and Its effect. The Journal of the Korean Institute of Information and Communication Engineering, 2015, 19, 2899-2904.	0.1	1

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73	Electrical Coupling of Monolithic 3D Inverters (M3INVs): MOSFET and Junctionless FET. Applied Sciences (Switzerland), 2021, 11, 277.	2.5	1
74	Monolithic 3D Inverter with Interface Charge: Parameter Extraction and Circuit Simulation. Applied Sciences (Switzerland), 2021, 11, 12151.	2.5	1
75	Comments on "A numerical analysis of the storage times of dynamic random-access memory cells incorporating ultrathin dielectrics". IEEE Transactions on Electron Devices, 2000, 47, 900-901.	3.0	0
76	Fabrication and characterization of GaAs/AlGaAs planar resonant tunneling transistor. , 2006, , .		0
77	New Adders Using Hybrid Circuit Consisting of Three-Gate Single-Electron Transistors (TG-SETs) and MOSFETs. Journal of Nanoscience and Nanotechnology, 2007, 7, 4120-4125.	0.9	0
78	Electrical characteristics of the back-gated bottom-up silicon nanowire field effect transistor. , 2008, , .		0
79	A compact model of fully-depleted surrounding-gate (SG) MOSFETs with a doped body. , 2008, , .		0
80	Power-, delay-, and emergency-efficient protocol for ubiquitous wireless sensor networks of silver town. , 2008, , .		0
81	Radio frequency pulse response of an in-plane-gate field effect transistor. Journal of Physics: Conference Series, 2008, 109, 012020.	0.4	0
82	Multi-Valued Logic Circuits Using Hybrid Circuit Consisting of Three Gates Single-Electron Transistors (TG-SETs) and MOSFETs. Journal of Nanoscience and Nanotechnology, 2008, 8, 4992-4998.	0.9	0
83	Simulation method for transmission-type radio-frequency single-electron transistor (RF-SET) operation by SPICE. Semiconductor Science and Technology, 2009, 24, 025020.	2.0	0
84	Analytic model of a silicon nanowire pH sensor. , 2010, , .		0
85	Modified proportional fair scheduling for Cognitive Radio networks. , 2012, , .		0
86	Workfunction Engineering of A Pocket Tunnel Field-Effect Transistor with A Dual Material Gate. Journal of the Korean Physical Society, 2018, 73, 308-313.	0.7	0
87	Electrical Coupling for Monolithic 3-D Integrated Circuit Consisting of Feedback Field-Effect Transistors. Journal of Nanoscience and Nanotechnology, 2021, 21, 4293-4297.	0.9	0
88	Interface Trap Charge Effects of Monolithic 3D Junctionless Field-Effect Transistors (JLFET) Inverter. Journal of Nanoscience and Nanotechnology, 2021, 21, 4252-4257.	0.9	0
89	Resonant tunneling through Quantum States of Enhancement Mode an In-Plane-Gate Quantum Dot Transistor. AIP Conference Proceedings, 2007, , .	0.4	0
90	Single-String Carbon Nanotube Field Effect Transistors Fabricated by Two-Step Dielectrophoresis. Japanese Journal of Applied Physics, 2012, 51, 06FE02.	1.5	0