# Chun-Hsing Shih

List of Publications by Year
in descending order



| 42 | 322 | 840776 11 | 888059 17 |
|---|---|---|---|
| papers | citations | h-index | g-index |

| 43 | 43 | 43 | 243 |
|---|---|---|---|
| all docs | docs citations | times ranked | citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Device operation and physical mechanism of asymmetric junctionless tunnel field-effect transistors designed to suppress coupled short-channel/short-drain effects and promote on-current switching for ultralow-voltage CMOS applications. Semiconductor Science and Technology, 2022, 37, 065007. | 2.0 | 1 |
| 2 | Device physics and design of hetero-gate dielectric tunnel field-effect transistors with different low/high-k EOT ratios. Applied Physics A: Materials Science and Processing, 2020, 126, 1. | 2.3 | 6 |
| 3 | Influence of hetero-gate dielectrics on short-channel effects in scaled tunnel field-effect transistors. Current Applied Physics, 2020, 20, 1342-1350. | 2.4 | 1 |
| 4 | Transverse Scaling of Schottky Barrier Charge-Trapping Cells for Energy-Efficient Applications. Crystals, 2020, 10, 1036. | 2.2 | 1 |
| 5 | Metallic Source/Drain Ge-Based Charge-Trapping Memory Cells. , 2019, , . | | 0 |
| 6 | Device physics and design of symmetrically doped tunnel field-effect transistors. Microelectronic Engineering, 2019, 216, 111061. | 2.4 | 4 |
| 7 | Effects of High Temperatures on Cell Reading, Programming, and Erasing of Schottky Barrier Charge-Trapping Memories. IEEE Transactions on Device and Materials Reliability, 2019, 19, 426-432. | 2.0 | 1 |
| 8 | Negative Capacitance in Short-Channel Tunnel Field-Effect Transistors. , 2019, , . | | 0 |
| 9 | Dependence of Short-Channel Effects on Semiconductor Bandgap in Tunnel Field-Effect Transistors. Journal of Physics: Conference Series, 2018, 1034, 012003. | 0.4 | 3 |
| 10 | Metallic Schottky barrier source/drain nanowire transistors using low-temperature microwave annealed nickel, ytterbium, and titanium silicidation. Materials Science in Semiconductor Processing, 2017, 70, 272-278. | 4.0 | 2 |
| 11 | Impact of gate-to-source/drain misalignments on source-side injection Schottky barrier charge-trapping memory cells evaluated using numerical programming-trapping iterations. Microelectronics Reliability, 2017, 74, 9-14. | 1.7 | 1 |
| 12 | Bandgap-dependent onset behavior of output characteristics in line-tunneling field-effect transistors. Journal of Computational Electronics, 2017, 16, 696-703. | 2.5 | 3 |
| 13 | Oxide thickness-dependent effects of source doping profile on the performance of single- and double-gate tunnel field-effect transistors. Superlattices and Microstructures, 2017, 102, 284-299. | 3.1 | 17 |
| 14 | Dopant-segregated metal source tunnel field-effect transistors with schottky barrier and band-to-band tunneling. , 2017, , . | | 0 |
| 15 | Different scalabilities of N- and P-type tunnel field-effect transistors with Si/SiGe heterojunctions. , 2016, , . | | 3 |
| 16 | Increasing drain voltage of low-bandgap tunnel field-effect transistors by drain engineering. , 2016, , . | | 3 |
| 17 | Short channel effects in tunnel field-effect transistors with different configurations of abrupt and graded Si/SiGe heterojunctions. Superlattices and Microstructures, 2016, 100, 857-866. | 3.1 | 12 |
| 18 | Drain-controlled ambipolar conduction and hot-hole injection in Schottky barrier charge-trapping memory cells. , 2015, , . | | 0 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Iterative programming analysis of dopant-segregated multibit/cell Schottky barrier charge-trapping memories. , 2015, , . | | 0 |
| 20 | Short-channel effect and device design of extremely scaled tunnel field-effect transistors. Microelectronics Reliability, 2015, 55, 31-37. | 1.7 | 14 |
| 21 | Thin Film Applications in Advanced Electron Devices. Advances in Materials Science and Engineering, 2014, 2014, 1-2. | 1.8 | 15 |
| 22 | Coupling of carriers injection and charges distribution in Schottky barrier charge-trapping memories using source-side electrons programming. Semiconductor Science and Technology, 2014, 29, 115006. | 2.0 | 12 |
| 23 | Design and Modeling of Line-Tunneling Field-Effect Transistors Using Low-Bandgap Semiconductors. IEEE Transactions on Electron Devices, 2014, 61, 1907-1913. | 3.0 | 24 |
| 24 | Effects of Dopant-Segregated Profiles on Schottky Barrier Charge-Trapping Flash Memories. IEEE Transactions on Electron Devices, 2014, 61, 1361-1368. | 3.0 | 3 |
| 25 | Sub-10-nm Asymmetric Junctionless Tunnel Field-Effect Transistors. IEEE Journal of the Electron Devices Society, 2014, 2, 128-132. | 2.1 | 11 |
| 26 | A Localized Two-Bit/Cell Nanowire SONOS Memory Using Schottky Barrier Source-Side Injected Programming. IEEE Nanotechnology Magazine, 2013, 12, 760-765. | 2.0 | 5 |
| 27 | Proper determination of tunnel model parameters for indirect band-to-band tunneling in compressively strained Si<inf>1−x</inf>Ge<inf>x</inf> TFETs. , 2013, , . | | 5 |
| 28 | Formation of arsenic segregated Ytterbium and Nickel silicide using microwave annealing. , 2013, , . | | 0 |
| 29 | Quantum confinement effect in strained-Si<inf>1−x</inf>Ge<inf>x</inf> double-gate tunnel field-effect transistors. , 2013, , . | | 2 |
| 30 | Fringing field and short channel effects in thin-body SOI MOSFETs with shallow source/drain. , 2013, , . | | 2 |
| 31 | Efficient and reliable Schottky barrier silicon nanowire charge-trapping flash memory. , 2012, , . | | 0 |
| 32 | Sub-10V 4-bit/cell Schottky barrier nanowire nonvolatile memory. , 2012, , . | | 1 |
| 33 | P-channel Schottky barrier nanowire SONOS memory with low-voltage operations and excellent reliability. , 2012, , . | | 0 |
| 34 | Reading Operation and Cell Scalability of Nonvolatile Schottky barrier Multibit Charge-Trapping Memory Cells. IEEE Transactions on Electron Devices, 2012, 59, 1599-1606. | 3.0 | 9 |
| 35 | Multilevel Schottky Barrier Nanowire SONOS Memory With Ambipolar n- and p-Channel Cells. IEEE Transactions on Electron Devices, 2012, 59, 1614-1620. | 3.0 | 17 |
| 36 | Sub-10-nm Tunnel Field-Effect Transistor With Graded Si/Ge Heterojunction. IEEE Electron Device Letters, 2011, 32, 1498-1500. | 3.9 | 76 |

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|---|---|---|---|
| 37 | On-current limitation of high-k gate insulator MOSFETs. , 2011, , . | | 1 |
| 38 | A Source-Side Injection Lucky Electron Model for Schottky Barrier Metalâ€“Oxideâ€“Semiconductor Devices. IEEE Electron Device Letters, 2011, 32, 1331-1333. | 3.9 | 16 |
| 39 | Schottky Barrier Silicon Nanowire SONOS Memory With Ultralow Programming and Erasing Voltages. IEEE Electron Device Letters, 2011, 32, 1477-1479. | 3.9 | 17 |
| 40 | Nonvolatile Schottky Barrier Multibit Cell With Source-Side Injected Programming and Reverse Drain-Side Hole Erasing. IEEE Transactions on Electron Devices, 2010, 57, 1774-1780. | 3.0 | 20 |
| 41 | Ambipolar conduction in recessed channel Schottky barrier MOSFETs. , 2010, , . | | 0 |
| 42 | Source-side injection Schottky barrier flash memory cells. Semiconductor Science and Technology, 2009, 24, 025013. | 2.0 | 14 |