

# Xuan Li

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/483105/publications.pdf>

Version: 2024-02-01

10  
papers

93  
citations

1684188

5  
h-index

1372567

10  
g-index

10  
all docs

10  
docs citations

10  
times ranked

70  
citing authors

#	ARTICLE	IF	CITATIONS
1	Reverse Bias Current Eliminated, Read-Separated, and Write-Enhanced Tunnel FET SRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 466-470.	3.0	1
2	Cascade Current Mirror to Improve Linearity and Consistency in SRAM In-Memory Computing. IEEE Journal of Solid-State Circuits, 2021, 56, 2550-2562.	5.4	24
3	Multiple Sharing 7T1R Nonvolatile SRAM With an Improved Read/Write Margin and Reliable Restore Yield. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 607-619.	3.1	14
4	In-Memory Computing With Double Word Lines and Three Read Ports for Four Operands. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1316-1320.	3.1	27
5	A single event upset tolerant latch with parallel nodes. IEICE Electronics Express, 2019, 16, 20190208-20190208.	0.8	5
6	An inverter chain with parallel output nodes for eliminating single-event transient pulse. IEICE Electronics Express, 2019, 16, 20181118-20181118.	0.8	1
7	Current mirror-based compensation circuit for multi-row read in-memory computing. Electronics Letters, 2019, 55, 1176-1178.	1.0	6
8	Read-decoupled 8T1R non-volatile SRAM with dual-mode option and high restore yield. Electronics Letters, 2019, 55, 519-521.	1.0	10
9	A dual-output hardening design of inverter chain for P-hit single-event transient pulse elimination. IEICE Electronics Express, 2018, 15, 20180604-20180604.	0.8	3
10	Self-compared bit-line pairs for eliminating effects of leakage current. Electronics Letters, 2017, 53, 1396-1398.	1.0	2