Xuan Li

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/483105/publications.pdf

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10	93	1684188 5	1372567 10
papers	citations	h-index	g-index

10	10	10	70
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	In-Memory Computing With Double Word Lines and Three Read Ports for Four Operands. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1316-1320.	3.1	27
2	Cascade Current Mirror to Improve Linearity and Consistency in SRAM In-Memory Computing. IEEE Journal of Solid-State Circuits, 2021, 56, 2550-2562.	5.4	24
3	Multiple Sharing 7T1R Nonvolatile SRAM With an Improved Read/Write Margin and Reliable Restore Yield. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 607-619.	3.1	14
4	Readâ€decoupled 8T1R nonâ€volatile SRAM with dualâ€mode option and high restore yield. Electronics Letters, 2019, 55, 519-521.	1.0	10
5	Current mirrorâ€based compensation circuit for multiâ€row read inâ€memory computing. Electronics Letters, 2019, 55, 1176-1178.	1.0	6
6	A single event upset tolerant latch with parallel nodes. IEICE Electronics Express, 2019, 16, 20190208-20190208.	0.8	5
7	A dual-output hardening design of inverter chain for P-hit single-event transient pulse elimination. IEICE Electronics Express, 2018, 15, 20180604-20180604.	0.8	3
8	Selfâ€compared bitâ€line pairs for eliminating effects of leakage current. Electronics Letters, 2017, 53, 1396-1398.	1.0	2
9	An inverter chain with parallel output nodes for eliminating single-event transient pulse. IEICE Electronics Express, 2019, 16, 20181118-20181118.	0.8	1
10	Reverse Bias Current Eliminated, Read-Separated, and Write-Enhanced Tunnel FET SRAM. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 466-470.	3.0	1