JÃ¼rgen Becker

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/4828958/publications.pdf

Version: 2024-02-01

110	663	1040056	940533
papers	citations	9	16
		h-index	g-index

115	115	115	518
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Lifecycle Management of Automotive Safety-Critical Over the Air Updates: A Systems Approach. IEEE Access, 2022, 10, 57696-57717.	4.2	5
2	A Hybrid Prototyping Framework in a Virtual Platform Centered Design and Verification Flow. IEEE Embedded Systems Letters, 2021, 13, 1-4.	1.9	2
3	Automatic Floorplanning and Standalone Generation of Bitstream-Level IP Cores. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 38-50.	3.1	3
4	Evaluation of Different Manual Placement Strategies to Ensure Uniformity of the V-FPGA. Lecture Notes in Computer Science, 2021, , 35-49.	1.3	1
5	Utilizing and Extending Trusted Execution Environment in Heterogeneous SoCs for a Pay-Per-Device IP Licensing Scheme. IEEE Transactions on Information Forensics and Security, 2021, 16, 2548-2563.	6.9	5
6	Moving Target and Implementation Diversity Based Countermeasures Against Side-Channel Attacks. Lecture Notes in Computer Science, 2021, , 188-202.	1.3	3
7	Transparent Near-Memory Computing with a Reconfigurable Processor. Lecture Notes in Computer Science, 2021, , 221-231.	1.3	1
8	Model Driven Development Process for a Service-oriented Industry 4.0 System. , 2020, , .		5
9	Fine Grained Control Flow Checking with Dedicated FPGA Monitors. , 2020, , .		0
10	A Network on Chip Adapter for Real-Time and Safety-Critical Applications. , 2019, , .		0
11	Secure Local Configuration of Intellectual Property Without a Trusted Third Party. Lecture Notes in Computer Science, 2019, , 137-146.	1.3	3
12	A Secure Framework with Remote Configuration of Intellectual Property. , 2019, , .		2
13	Reconfigurable FPGA-Based Channelization Using Polyphase Filter Banks for Quantum Computing Systems. Lecture Notes in Computer Science, 2018, , 615-626.	1.3	2
14	Scenario-based development of an industry 4.0 domain description language for a plant architecture. , 2018, , .		3
15	A Content - Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique. , 2018, , .		2
16	OpenCL-based Virtual Prototyping and Simulation of Many-Accelerator Architectures. Transactions on Embedded Computing Systems, 2018, 17, 1-27.	2.9	1
17	The ARAMiS Project Initiative. Lecture Notes in Computer Science, 2018, , 685-699.	1.3	0
18	A WCET-aware parallel programming model for predictability enhanced multi-core architectures. , 2018, , .		3

#	Article	IF	Citations
19	Advances in Avionic Platforms: Multi-core Systems. , 2018, , 17-27.		0
20	WCET-aware parallelization of model-based applications for multi-cores: The ARGO approach. , 2017, , .		9
21	A Timing Synchronizer System for Beam Test Setups Requiring Galvanic Isolation. IEEE Transactions on Nuclear Science, 2017, 64, 1975-1982.	2.0	0
22	Efficient task spawning for shared memory and message passing in many-core architectures. Journal of Systems Architecture, 2017, 77, 72-82.	4.3	3
23	Auto-SI: An adaptive reconfigurable processor with run-time loop detection and acceleration. , 2017, , .		5
24	A reconfigurable high-speed spiral FIR filter architecture. , 2017, , .		0
25	Providing fault tolerance through invasive computing. IT - Information Technology, 2016, 58, 309-328.	0.9	3
26	A variable FPGA based generic QAM transmitter with scalable mixed time and frequency domain signal processing. , 2016, , .		0
27	Power Management Controller for Online Power Saving in Network-on-Chips. , 2016, , .		1
28	An OpenCL-based framework for rapid virtual prototyping of heterogeneous architectures. , 2016, , .		0
29	Adaptive Bandwidth Router for 3D Network-on-Chips. Lecture Notes in Computer Science, 2016, , 352-360.	1.3	0
30	Cloud-based remote virtual prototyping platform for embedded control applications: Cloud-based infrastructure for large-scale embedded hardware-related programming laboratories. , 2016, , .		6
31	Programmable Logic as Device Virtualization Layer in Heterogeneous Multicore Architectures. Lecture Notes in Computer Science, 2016, , 273-286.	1.3	0
32	A Content Adapted FPGA Memory Architecture with Pattern Recognition Capability for L1 Track Triggering in the LHC Environment. , 2016, , .		13
33	An introductory microcontroller programming laboratory course for first-year students. International Journal of Electrical Engineering and Education, 2016, 53, 99-113.	0.8	4
34	High-Speed Medical Imaging in 3D Ultrasound Computer Tomography. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 455-467.	5.6	17
35	Adaptive Cache Structures. Lecture Notes in Computer Science, 2016, , 87-99.	1.3	3
36	A Dynamic Cache Architecture for Efficient Memory Resource Allocation in Many-Core Systems. Lecture Notes in Computer Science, 2016, , 343-351.	1.3	0

#	Article	IF	Citations
37	Designing applications for heterogeneous many-core architectures with the FlexTiles Platform. , 2015, , .		9
38	A power estimation technique for cycle-accurate higher-abstraction SystemC-based CPU models. , 2015, , .		4
39	A Framework for Multi-FPGA Interconnection using Multi Gigabit Transceivers. , 2015, , .		3
40	Parametric design space exploration for optimizing QAM based high-speed communication. , 2015, , .		2
41	RAW Introduction and Committees. , 2015, , .		0
42	Virtual prototyping of heterogeneous dynamic platforms using Open Virtual Platforms. , 2015, , .		0
43	Evaluation of analog and digital signal processing on PSoC architecture with DCT as use case: Comparison of an analog and software based implementation of the digital cosine transform on a Programmable System on Chip. , 2015, , .		0
44	Design of an embedded UWB hardware platform for navigation in GPS denied environments. , 2015, , .		18
45	Adaptive algorithm and tool flow for accelerating SystemC on many-core architectures. Microprocessors and Microsystems, 2015, 39, 1063-1075.	2.8	4
46	Fault-tolerant communication in invasive networks on chip. , 2015, , .		3
47	Software-in-the-Loop simulation of embedded control applications based on Virtual Platforms. , 2015, , .		10
48	Network Interface with Task Spawning Support for NoC-Based DSM Architectures. Lecture Notes in Computer Science, 2015, , 186-198.	1.3	3
49	TEAChER: TEach AdvanCEd Reconfigurable Architectures and Tools. Lecture Notes in Computer Science, 2015, , 103-114.	1.3	0
50	A V2X Message Evaluation Methodology and Cross-Domain Modelling of Safety Applications in V2X-enabled E/E-Architectures. , 2015, , .		2
51	A Hierarchical Architecture Description for Flexible Multicore System Simulation. , 2014, , .		1
52	CAP. , 2014, , .		8
53	Architectural measures against radiation effects in multicore SoC for safety critical applications. , 2014, , .		3
54	Hardware/software debugging of large scale many-core architectures. , 2014, , .		2

#	Article	IF	Citations
55	Adaptive Algorithm and Tool Flow for Accelerating SystemC on Many-Core Architectures. , 2014, , .		8
56	A comprehensive comparison of GPU- and FPGA-based acceleration of reflection image reconstruction for 3D ultrasound computer tomography. Journal of Real-Time Image Processing, 2014, 9, 159-170.	3.5	25
57	SmartLoCore: A Concept for an Adaptive Power-Aware Localization Processor. , 2014, , .		0
58	Hardware virtualization support for shared resources in mixed-criticality multicore systems. , 2014, , .		4
59	Novel Techniques for Smart Adaptive Multiprocessor SoCs. IEEE Transactions on Computers, 2014, , 1-1.	3.4	1
60	Towards Dynamic Cache and Bandwidth Invasion. Lecture Notes in Computer Science, 2014, , 97-107.	1.3	1
61	Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors. , 2014, , .		9
62	Profile-Guided Compilation of Scilab Algorithms for Multiprocessor Systems. Lecture Notes in Computer Science, 2014, , 330-336.	1.3	0
63	HETA: Hybrid Error-Detection Technique Using Assertions. IEEE Transactions on Nuclear Science, 2013, 60, 2805-2812.	2.0	37
64	Reliable and adaptive network-on-chip architectures for cyber physical systems. Transactions on Embedded Computing Systems, 2013, 12, 1-21.	2.9	4
65	Improving parallel MPSoC simulation performance by exploiting dynamic routing delay prediction. , 2013, , .		0
66	Rerouting: Scalable NoC self-optimization by distributed hardware-based connection reallocation. , 2013, , .		5
67	Hybrid Interconnect Design for Heterogeneous Hardware Accelerators. , 2013, , .		7
68	Hardware Supported Adaptive Data Collection for Networks on Chip. , 2013, , .		3
69	A platform-independent runtime methodology for mapping multiple applications onto FPGAs through resource virtualization. , 2013, , .		3
70	LImbiC: An adaptable architecture description language model for developing an application-specific image processor. , 2013, , .		1
71	Efficient memory access in 2D Mesh NoC architectures using high bandwidth routers. , 2013, , .		4
72	Providing multiple hard latency and throughput guarantees for packet switching networks on chip. Computers and Electrical Engineering, 2013, 39, 2603-2622.	4.8	37

#	Article	IF	Citations
73	Development and Evaluation of Distributed Simulation of Embedded Systems Using Ptolemy and HLA. , 2013, , .		15
74	JITPR. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1-12.	2.5	5
75	Virtual networks -- distributed communication resource management. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1-14.	2.5	5
76	Simplify: A Framework for Enabling Fast Functional/Behavioral Validation of Multiprocessor Architectures in the Cloud. , 2013, , .		3
77	A novel system on chip for software-defined, high-speed OFDM signal processing. , 2013, , .		4
78	AUTO-GS: Self-Optimization of NoC Traffic through Hardware Managed Virtual Connections. , 2013, , .		1
79	An FPGA-based multi-core approach for pipelining computing stages. , 2013, , .		4
80	JITPR. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1.	2.5	7
81	Embedded Systems Start-Up Under Timing Constraints on Modern FPGAs. , 2013, , 149-172.		0
82	A Fault Tolerant Approach to Detect Transient Faults in Microprocessors Based on a Non-Intrusive Reconfigurable Hardware. IEEE Transactions on Nuclear Science, 2012, 59, 1117-1124.	2.0	24
83	Hardware-assisted Decentralized Resource Management for Networks on Chip with QoS. , 2012, , .		3
84	A Scalable NoC Router Design Providing QoS Support Using Weighted Round Robin Scheduling. , 2012, , .		21
85	Determination of on-chip temperature gradients on reconfigurable hardware. , 2012, , .		6
86	Asynchronous parallel MPSoC simulation on the Single-Chip Cloud Computer. , 2012, , .		11
87	Adaptive processor architecture - invited paper. , 2012, , .		1
88	LISPARC: Using an architecture description language approach for modelling an adaptive processor microarchitecture. , 2012, , .		5
89	Exploration of Uninitialized Configuration Memory Space for Intrinsic Identification of Xilinx Virtex-5 FPGA Devices. International Journal of Reconfigurable Computing, 2012, 2012, 1-10.	0.2	1
90	Efficient Execution of Networked MPSoC Models by Exploiting Multiple Platform Levels. International Journal of Reconfigurable Computing, 2012, 2012, 1-13.	0.2	0

#	Article	IF	Citations
91	HoneyComb: An Application-Driven Online Adaptive Reconfigurable Hardware Architecture. International Journal of Reconfigurable Computing, 2012, 2012, 1-17.	0.2	3
92	Adaptive Multiclient Network-on-Chip Memory Core: Hardware Architecture, Software Abstraction Layer, and Application Exploration. International Journal of Reconfigurable Computing, 2012, 2012, 1-14.	0.2	3
93	A Framework for Exploration of Parallel SystemC Simulation on the Single-chip Cloud Computer. , 2012, , .		6
94	Acceleration of image reconstruction in 3D ultrasound computer tomography: An evaluation of CPU, GPU and FPGA computing. , 2011, , .		7
95	Heterogeneous and runtime parameterizable Star-Wheels Network-on-Chip. , 2011, , .		11
96	Implementation of an ultra-high speed 256-point FFT for Xilinx Virtex-6 devices. , 2011, , .		9
97	A heterogeneous SoC architecture with embedded virtual FPGA cores and runtime Core Fusion. , 2011, , .		8
98	Evaluation of the Reconfiguration of the Data Acquisition System for 3D USCT. International Journal of Reconfigurable Computing, 2011, 2011, 1-9.	0.2	6
99	Reconfiguration Techniques for Self-X Power and Performance Management on Xilinx Virtex-II/Virtex-II-Pro FPGAs. International Journal of Reconfigurable Computing, 2011, 2011, 1-12.	0.2	3
100	Prime Field ECDSA Signature Processing for Reconfigurable Embedded Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-12.	0.2	24
101	Exploration of the Power-Performance Tradeoff through Parameterization of FPGA-Based Multiprocessor Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-17.	0.2	5
102	A Security Scheme for Dependable Key Insertion in Mobile Embedded Devices. International Journal of Reconfigurable Computing, 2011, 2011, 1-19.	0.2	3
103	Operating System for Runtime Reconfigurable Multiprocessor Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-16.	0.2	24
104	FPGA-Based Runtime Adaptive Multiprocessor Approach for Embedded High Performance Computing Applications. , 2010, , .		6
105	Adaptive real-time image processing exploiting two dimensional reconfigurable architecture. Journal of Real-Time Image Processing, 2009, 4, 109-125.	3.5	17
106	Data Reallocation by Exploiting FPGA Configuration Mechanisms. Lecture Notes in Computer Science, 2008, , 312-317.	1.3	10
107	Physical Configuration On-Line Visualization of Xilinx Virtex-II FPGAs. , 2007, , .		12
108	MORPHEUS: Heterogeneous Reconfigurable Computing. , 2007, , .		55

#	Article	IF	Citations
109	New Adaptive Multi-grained Hardware Architecture for Processing of Dynamic Function Patterns (Neue adaptive multi-granulare Hardwarearchitektur). IT - Information Technology, 2007, 49, 165-173.	0.9	5
110	V-FPGAs: Increasing Performance with Manual Placement, Timing Extraction and Extended Timing Modeling. Journal of Signal Processing Systems, 0, , .	2.1	1