

Jürgen Becker

List of Publications by Year in descending order

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Version: 2024-02-01

110
papers

663
citations

1040056

9
h-index

940533

16
g-index

115
all docs

115
docs citations

115
times ranked

518
citing authors

#	ARTICLE	IF	CITATIONS
1	MORPHEUS: Heterogeneous Reconfigurable Computing. , 2007, , .		55
2	HETA: Hybrid Error-Detection Technique Using Assertions. IEEE Transactions on Nuclear Science, 2013, 60, 2805-2812.	2.0	37
3	Providing multiple hard latency and throughput guarantees for packet switching networks on chip. Computers and Electrical Engineering, 2013, 39, 2603-2622.	4.8	37
4	A comprehensive comparison of GPU- and FPGA-based acceleration of reflection image reconstruction for 3D ultrasound computer tomography. Journal of Real-Time Image Processing, 2014, 9, 159-170.	3.5	25
5	Prime Field ECDSA Signature Processing for Reconfigurable Embedded Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-12.	0.2	24
6	Operating System for Runtime Reconfigurable Multiprocessor Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-16.	0.2	24
7	A Fault Tolerant Approach to Detect Transient Faults in Microprocessors Based on a Non-Intrusive Reconfigurable Hardware. IEEE Transactions on Nuclear Science, 2012, 59, 1117-1124.	2.0	24
8	A Scalable NoC Router Design Providing QoS Support Using Weighted Round Robin Scheduling. , 2012, , .		21
9	Design of an embedded UWB hardware platform for navigation in GPS denied environments. , 2015, , .		18
10	Adaptive real-time image processing exploiting two dimensional reconfigurable architecture. Journal of Real-Time Image Processing, 2009, 4, 109-125.	3.5	17
11	High-Speed Medical Imaging in 3D Ultrasound Computer Tomography. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 455-467.	5.6	17
12	Development and Evaluation of Distributed Simulation of Embedded Systems Using Ptolemy and HLA. , 2013, , .		15
13	A Content Adapted FPGA Memory Architecture with Pattern Recognition Capability for L1 Track Triggering in the LHC Environment. , 2016, , .		13
14	Physical Configuration On-Line Visualization of Xilinx Virtex-II FPGAs. , 2007, , .		12
15	Heterogeneous and runtime parameterizable Star-Wheels Network-on-Chip. , 2011, , .		11
16	Asynchronous parallel MPSoC simulation on the Single-Chip Cloud Computer. , 2012, , .		11
17	Software-in-the-Loop simulation of embedded control applications based on Virtual Platforms. , 2015, , .		10
18	Data Reallocation by Exploiting FPGA Configuration Mechanisms. Lecture Notes in Computer Science, 2008, , 312-317.	1.3	10

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19	Implementation of an ultra-high speed 256-point FFT for Xilinx Virtex-6 devices. , 2011, , .		9
20	Designing applications for heterogeneous many-core architectures with the FlexTiles Platform. , 2015, , .		9
21	WCET-aware parallelization of model-based applications for multi-cores: The ARGO approach. , 2017, , .		9
22	Hybrid Fault Tolerance Techniques to Detect Transient Faults in Embedded Processors. , 2014, , .		9
23	A heterogeneous SoC architecture with embedded virtual FPGA cores and runtime Core Fusion. , 2011, , .		8
24	CAP. , 2014, , .		8
25	Adaptive Algorithm and Tool Flow for Accelerating SystemC on Many-Core Architectures. , 2014, , .		8
26	Acceleration of image reconstruction in 3D ultrasound computer tomography: An evaluation of CPU, GPU and FPGA computing. , 2011, , .		7
27	Hybrid Interconnect Design for Heterogeneous Hardware Accelerators. , 2013, , .		7
28	JITPR. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1.	2.5	7
29	FPGA-Based Runtime Adaptive Multiprocessor Approach for Embedded High Performance Computing Applications. , 2010, , .		6
30	Evaluation of the Reconfiguration of the Data Acquisition System for 3D USCT. International Journal of Reconfigurable Computing, 2011, 2011, 1-9.	0.2	6
31	Determination of on-chip temperature gradients on reconfigurable hardware. , 2012, , .		6
32	Cloud-based remote virtual prototyping platform for embedded control applications: Cloud-based infrastructure for large-scale embedded hardware-related programming laboratories. , 2016, , .		6
33	A Framework for Exploration of Parallel SystemC Simulation on the Single-chip Cloud Computer. , 2012, , .		6
34	Exploration of the Power-Performance Tradeoff through Parameterization of FPGA-Based Multiprocessor Systems. International Journal of Reconfigurable Computing, 2011, 2011, 1-17.	0.2	5
35	LISPARC: Using an architecture description language approach for modelling an adaptive processor microarchitecture. , 2012, , .		5
36	Rerouting: Scalable NoC self-optimization by distributed hardware-based connection reallocation. , 2013, , .		5

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37	JITPR. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1-12.	2.5	5
38	Virtual networks – distributed communication resource management. ACM Transactions on Reconfigurable Technology and Systems, 2013, 6, 1-14.	2.5	5
39	Auto-SI: An adaptive reconfigurable processor with run-time loop detection and acceleration. , 2017, , .		5
40	Model Driven Development Process for a Service-oriented Industry 4.0 System. , 2020, , .		5
41	Utilizing and Extending Trusted Execution Environment in Heterogeneous SoCs for a Pay-Per-Device IP Licensing Scheme. IEEE Transactions on Information Forensics and Security, 2021, 16, 2548-2563.	6.9	5
42	New Adaptive Multi-grained Hardware Architecture for Processing of Dynamic Function Patterns (Neue adaptive multi-granulare Hardwarearchitektur). IT - Information Technology, 2007, 49, 165-173.	0.9	5
43	Lifecycle Management of Automotive Safety-Critical Over the Air Updates: A Systems Approach. IEEE Access, 2022, 10, 57696-57717.	4.2	5
44	Reliable and adaptive network-on-chip architectures for cyber physical systems. Transactions on Embedded Computing Systems, 2013, 12, 1-21.	2.9	4
45	Efficient memory access in 2D Mesh NoC architectures using high bandwidth routers. , 2013, , .		4
46	A novel system on chip for software-defined, high-speed OFDM signal processing. , 2013, , .		4
47	An FPGA-based multi-core approach for pipelining computing stages. , 2013, , .		4
48	Hardware virtualization support for shared resources in mixed-criticality multicore systems. , 2014, , .		4
49	A power estimation technique for cycle-accurate higher-abstraction SystemC-based CPU models. , 2015, , .		4
50	Adaptive algorithm and tool flow for accelerating SystemC on many-core architectures. Microprocessors and Microsystems, 2015, 39, 1063-1075.	2.8	4
51	An introductory microcontroller programming laboratory course for first-year students. International Journal of Electrical Engineering and Education, 2016, 53, 99-113.	0.8	4
52	Reconfiguration Techniques for Self-X Power and Performance Management on Xilinx Virtex-II/Virtex-II-Pro FPGAs. International Journal of Reconfigurable Computing, 2011, 2011, 1-12.	0.2	3
53	A Security Scheme for Dependable Key Insertion in Mobile Embedded Devices. International Journal of Reconfigurable Computing, 2011, 2011, 1-19.	0.2	3
54	Hardware-assisted Decentralized Resource Management for Networks on Chip with QoS. , 2012, , .		3

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55	HoneyComb: An Application-Driven Online Adaptive Reconfigurable Hardware Architecture. International Journal of Reconfigurable Computing, 2012, 2012, 1-17.	0.2	3
56	Adaptive Multiclient Network-on-Chip Memory Core: Hardware Architecture, Software Abstraction Layer, and Application Exploration. International Journal of Reconfigurable Computing, 2012, 2012, 1-14.	0.2	3
57	Hardware Supported Adaptive Data Collection for Networks on Chip. , 2013, , .		3
58	A platform-independent runtime methodology for mapping multiple applications onto FPGAs through resource virtualization. , 2013, , .		3
59	Simplify: A Framework for Enabling Fast Functional/Behavioral Validation of Multiprocessor Architectures in the Cloud. , 2013, , .		3
60	Architectural measures against radiation effects in multicore SoC for safety critical applications. , 2014, , .		3
61	A Framework for Multi-FPGA Interconnection using Multi Gigabit Transceivers. , 2015, , .		3
62	Fault-tolerant communication in invasive networks on chip. , 2015, , .		3
63	Providing fault tolerance through invasive computing. IT - Information Technology, 2016, 58, 309-328.	0.9	3
64	Efficient task spawning for shared memory and message passing in many-core architectures. Journal of Systems Architecture, 2017, 77, 72-82.	4.3	3
65	Scenario-based development of an industry 4.0 domain description language for a plant architecture. , 2018, , .		3
66	A WCET-aware parallel programming model for predictability enhanced multi-core architectures. , 2018, , .		3
67	Automatic Floorplanning and Standalone Generation of Bitstream-Level IP Cores. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 38-50.	3.1	3
68	Moving Target and Implementation Diversity Based Countermeasures Against Side-Channel Attacks. Lecture Notes in Computer Science, 2021, , 188-202.	1.3	3
69	Secure Local Configuration of Intellectual Property Without a Trusted Third Party. Lecture Notes in Computer Science, 2019, , 137-146.	1.3	3
70	Network Interface with Task Spawning Support for NoC-Based DSM Architectures. Lecture Notes in Computer Science, 2015, , 186-198.	1.3	3
71	Adaptive Cache Structures. Lecture Notes in Computer Science, 2016, , 87-99.	1.3	3
72	Hardware/software debugging of large scale many-core architectures. , 2014, , .		2

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73	Parametric design space exploration for optimizing QAM based high-speed communication. , 2015, , .		2
74	Reconfigurable FPGA-Based Channelization Using Polyphase Filter Banks for Quantum Computing Systems. Lecture Notes in Computer Science, 2018, , 615-626.	1.3	2
75	A Content - Adapted FPGA Memory Architecture with Pattern Recognition Capability and Interval Compressing Technique. , 2018, , .		2
76	A Hybrid Prototyping Framework in a Virtual Platform Centered Design and Verification Flow. IEEE Embedded Systems Letters, 2021, 13, 1-4.	1.9	2
77	A V2X Message Evaluation Methodology and Cross-Domain Modelling of Safety Applications in V2X-enabled E/E-Architectures. , 2015, , .		2
78	A Secure Framework with Remote Configuration of Intellectual Property. , 2019, , .		2
79	Adaptive processor architecture - invited paper. , 2012, , .		1
80	Exploration of Uninitialized Configuration Memory Space for Intrinsic Identification of Xilinx Virtex-5 FPGA Devices. International Journal of Reconfigurable Computing, 2012, 2012, 1-10.	0.2	1
81	ImbiC: An adaptable architecture description language model for developing an application-specific image processor. , 2013, , .		1
82	AUTO-GS: Self-Optimization of NoC Traffic through Hardware Managed Virtual Connections. , 2013, , .		1
83	A Hierarchical Architecture Description for Flexible Multicore System Simulation. , 2014, , .		1
84	Novel Techniques for Smart Adaptive Multiprocessor SoCs. IEEE Transactions on Computers, 2014, , 1-1.	3.4	1
85	Power Management Controller for Online Power Saving in Network-on-Chips. , 2016, , .		1
86	OpenCL-based Virtual Prototyping and Simulation of Many-Accelerator Architectures. Transactions on Embedded Computing Systems, 2018, 17, 1-27.	2.9	1
87	Evaluation of Different Manual Placement Strategies to Ensure Uniformity of the V-FPGA. Lecture Notes in Computer Science, 2021, , 35-49.	1.3	1
88	Transparent Near-Memory Computing with a Reconfigurable Processor. Lecture Notes in Computer Science, 2021, , 221-231.	1.3	1
89	Towards Dynamic Cache and Bandwidth Invasion. Lecture Notes in Computer Science, 2014, , 97-107.	1.3	1
90	V-FPGAs: Increasing Performance with Manual Placement, Timing Extraction and Extended Timing Modeling. Journal of Signal Processing Systems, 0, , .	2.1	1

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91	Efficient Execution of Networked MPSoC Models by Exploiting Multiple Platform Levels. International Journal of Reconfigurable Computing, 2012, 2012, 1-13.	0.2	0
92	Improving parallel MPSoC simulation performance by exploiting dynamic routing delay prediction. , 2013, , .		0
93	SmartLoCore: A Concept for an Adaptive Power-Aware Localization Processor. , 2014, , .		0
94	RAW Introduction and Committees. , 2015, , .		0
95	Virtual prototyping of heterogeneous dynamic platforms using Open Virtual Platforms. , 2015, , .		0
96	Evaluation of analog and digital signal processing on PSoC architecture with DCT as use case: Comparison of an analog and software based implementation of the digital cosine transform on a Programmable System on Chip. , 2015, , .		0
97	A variable FPGA based generic QAM transmitter with scalable mixed time and frequency domain signal processing. , 2016, , .		0
98	An OpenCL-based framework for rapid virtual prototyping of heterogeneous architectures. , 2016, , .		0
99	Adaptive Bandwidth Router for 3D Network-on-Chips. Lecture Notes in Computer Science, 2016, , 352-360.	1.3	0
100	Programmable Logic as Device Virtualization Layer in Heterogeneous Multicore Architectures. Lecture Notes in Computer Science, 2016, , 273-286.	1.3	0
101	A Timing Synchronizer System for Beam Test Setups Requiring Galvanic Isolation. IEEE Transactions on Nuclear Science, 2017, 64, 1975-1982.	2.0	0
102	A reconfigurable high-speed spiral FIR filter architecture. , 2017, , .		0
103	The ARAMiS Project Initiative. Lecture Notes in Computer Science, 2018, , 685-699.	1.3	0
104	A Network on Chip Adapter for Real-Time and Safety-Critical Applications. , 2019, , .		0
105	Embedded Systems Start-Up Under Timing Constraints on Modern FPGAs. , 2013, , 149-172.		0
106	Profile-Guided Compilation of Scilab Algorithms for Multiprocessor Systems. Lecture Notes in Computer Science, 2014, , 330-336.	1.3	0
107	TEACHER: TEach AdvanCEd Reconfigurable Architectures and Tools. Lecture Notes in Computer Science, 2015, , 103-114.	1.3	0
108	A Dynamic Cache Architecture for Efficient Memory Resource Allocation in Many-Core Systems. Lecture Notes in Computer Science, 2016, , 343-351.	1.3	0

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109	Advances in Avionic Platforms: Multi-core Systems. , 2018, , 17-27.		0
110	Fine Grained Control Flow Checking with Dedicated FPGA Monitors. , 2020, , .		0