Todor Stefanov

List of Publications by Year in descending order

36 papers	395 citations	1307594 7 h-index	1281871 11 g-index
36 all docs	36 docs citations	36 times ranked	272 citing authors

#	ARTICLE	IF	CITATIONS
1	Scenario Based Run-Time Switching for Adaptive CNN-Based Applications at the Edge. Transactions on Embedded Computing Systems, 2022, 21, 1-33.	2.9	3
2	ALOHA: A Unified Platform-Aware Evaluation Method for CNNs Execution on Heterogeneous Systems at the Edge. IEEE Access, 2021, 9, 133289-133308.	4.2	7
3	DAEDALUS Framework for High-Level Synthesis: Past, Present and Future. , 2021, , .		1
4	Combining Task- and Data-Level Parallelism for High-Throughput CNN Inference on Embedded CPUs-GPUs MPSoCs. Lecture Notes in Computer Science, 2020, , 18-35.	1.3	20
5	Buffer Sizes Reduction for Memory-efficient CNN Inference on Mobile and Embedded Devices. , 2020, , .		3
6	Enabling Cognitive Autonomy on Small Drones by Efficient On-Board Embedded Computing: An ORB-SLAM2 Case Study. , 2019, , .		4
7	Surf-Bless. , 2019, , .		2
8	Optimization and deployment of CNNs at the edge. , 2019, , .		10
9	Hard Real-Time Scheduling of Streaming Applications Modeled as Cyclic CSDF Graphs. , 2019, , .		7
10	EVC-Based Power Gating Approach to Achieve Low-Power and High Performance NoC. , 2019, , .		1
11	Scheduling Analysis of Imprecise Mixed-Criticality Real-Time Tasks. IEEE Transactions on Computers, 2018, 67, 975-991.	3.4	34
12	Utilization-Based Scheduling of Flexible Mixed-Criticality Real-Time Tasks. IEEE Transactions on Computers, 2018, 67, 543-558.	3.4	31
13	Architecture-aware design and implementation of CNN algorithms for embedded inference: the ALOHA project. , 2018, , .		1
14	Modeling, Analysis, and Hard Real-Time Scheduling of Adaptive Streaming Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2636-2648.	2.7	4
15	Resource Optimization for Real-Time Streaming Applications Using Task Replication. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2755-2767.	2.7	4
16	A Simple Convolutional Neural Network for Accurate P300 Detection and Character Spelling in Brain Computer Interface. , 2018, , .		30
17	A Novel Approach to Reduce Packet Latency Increase Caused by Power Gating in Network-on-Chip. , 2017, , .		8
18	Energy-efficient scheduling of throughput-constrained streaming applications by periodic mode switching. , 2017, , .		1

#	Article	IF	Citations
19	Parametrized system level design: Real-time X-Ray image processing case study. , 2016, , .		0
20	Reconfigurable cache for real-time MPSoCs: Scheduling and implementation. Microprocessors and Microsystems, 2016, 42, 200-214.	2.8	4
21	Energy-Efficient Scheduling of Real-Time Tasks on Heterogeneous Multicores Using Task Splitting. , 2016, , .		13
22	Energy-efficient mapping of real-time applications on heterogeneous MPSoCs using task replication. , 2016, , .		12
23	Resource optimization for CSDF-modeled streaming applications with latency constraints. , 2014, , .		1
24	System-level scheduling of real-time streaming applications using a semi-partitioned approach. , 2014, , .		3
25	Resource optimization for CSDF-modeled streaming applications with latency constraints. , 2014, , .		0
26	System-level scheduling of real-time streaming applications using a semi-partitioned approach. , 2014, , .		3
27	An accurate energy model for streaming applications mapped on MPSoC platforms. , 2013, , .		2
28	A system-level approach to adaptivity and fault-tolerance in NoC-based MPSoCs: The MADNESS project. Microprocessors and Microsystems, 2013, 37, 515-529.	2.8	13
29	A methodology for automated design of hard-real-time embedded streaming systems. , 2012, , .		14
30	Mapping of streaming applications considering alternative application specifications (Extended) Tj ETQq0 0 0 rgBT /Overlock 10 Tf 50 30		0
31	Adaptivity Support for MPSoCs Based on Process Migration in Polyhedral Process Networks. VLSI Design, 2012, 2012, 1-17.	0.5	15
32	Automatic derivation of polyhedral process networks from while-loop affine programs. , 2011, , .		7
33	Throughput modeling to evaluate process merging transformations in polyhedral process networks. , 2010, , .		16
34	Translating affine nested-loop programs with dynamic loop bounds into Polyhedral Process Networks. , 2010, , .		6
35	Systematic and Automated Multiprocessor System Design, Programming, and Implementation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 542-555.	2.7	107
36	Affine Nested Loop Programs and their Binary Parameterized Dataflow Graph Counterparts. , 2006, , .		8