Felice Crupi

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

153 papers	2,361 citations	25 h-index	39 g-index
168 ext. papers	2,910 ext. citations	2.6 avg, IF	4.87 L-index

#	Paper	IF	Citations
153	Static CMOS Physically Unclonable Function Based on 4T Voltage Divider With 0.6%-1.5% Bit Instability at 0.4-1.8 V Operation in 180 nm. *IEEE Journal of Solid-State Circuits*, **2022**, 1-12	5.5	3
152	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. *Solid-State Electronics*, **2022**, 194, 108315	1.7	
151	Smart Material Implication Using Spin-Transfer Torque Magnetic Tunnel Junctions for Logic-in-Memory Computing. *Solid-State Electronics*, **2022**, 108390	1.7	
150	Assessment of paper-based MoS2 FET for Physically Unclonable Functions. *Solid-State Electronics*, **2022**, 194, 108391	1.7	1
149	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 1393-1397	3.5	1
148	A Low-Voltage, Low-Power Reconfigurable Current-Mode Softmax Circuit for Analog Neural Networks. *Electronics (Switzerland)*, **2021**, 10, 1004	2.6	2
147	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. *IEEE Transactions on Magnetics*, **2021**, 57, 1-6	2	9
146	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. *IEEE Nanotechnology Magazine*, **2021**, 20, 123-128	2.6	11
145	A 0.05 mm2, 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 1-1	3.5	3
144	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2021**, 68, 3038-3042	3.5	3
143	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. *Solid-State Electronics*, **2021**, 184, 108090	1.7	7
142	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 3134-3144	5.5	9
141	STT-MTJ Based Smart Implication for Energy-Efficient Logic-in-Memory Computing. *Solid-State Electronics*, **2021**, 184, 108065	1.7	3
140	Assessment of 2D-FET Based Digital and Analog Circuits on Paper. *Solid-State Electronics*, **2021**, 185, 108063	1.7	1
139	BTI saturation and universal relaxation in SiC power MOSFETs. *Microelectronics Reliability*, **2020**, 109, 113642	1.2	1
138	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. *The Integration VLSI Journal*, **2020**, 71, 56-69	1.4	11
137	Reliability Assessment of AlGaN/GaN Schottky Barrier Diodes Under ON-State Stress. *IEEE Transactions on Device and Materials Reliability*, **2020**, 20, 167-171	1.6	2

136	Impact of Scaling on Physical Unclonable Function Based on Spin□Orbit Torque. *IEEE Magnetics Letters*, **2020**, 11, 1-5	1.6	1
135	Compact Modeling of Perpendicular STT-MTJs With Double Reference Layers. *IEEE Nanotechnology Magazine*, **2019**, 18, 1063-1070	2.6	13
134	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. *Microelectronic Engineering*, **2019**, 215, 111009	2.5	15
133	Numerical simulations of hole carrier selective contacts in p-type c-Si solar cells. *Solar Energy Materials and Solar Cells*, **2019**, 200, 109937	6.4	16
132	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs **2019**,		3
131	Making IoT Services Accountable: A Solution Based on Blockchain and Physically Unclonable Functions. *Lecture Notes in Computer Science*, **2019**, 294-305	0.9	2
130	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops **2019**,		1
129	Influence of GaN- and Si3N4-Passivation Layers on the Performance of AlGaN/GaN Diodes With a Gated Edge Termination. *IEEE Transactions on Electron Devices*, **2019**, 66, 883-889	2.9	3
128	A portable class of 3-transistor current references with low-power sub-0.5□V operation. *International Journal of Circuit Theory and Applications*, **2018**, 46, 779-795	2	7
127	Diagnosis of phosphorus monolayer doping in silicon based on nanowire electrical characterisation. *Journal of Applied Physics*, **2018**, 123, 125701	2.5	12
126	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 1086-1095	3.9	26
125	Reliability Improvements in AlGaN/GaN Schottky Barrier Diodes With a Gated Edge Termination. *IEEE Transactions on Electron Devices*, **2018**, 65, 1765-1770	2.9	14
124	Digital and analog TFET circuits: Design and benchmark. *Solid-State Electronics*, **2018**, 146, 50-65	1.7	40
123	An Ultralow-Voltage Energy-Efficient Level Shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 61-65	3.5	38
122	Single Defect Discharge Events in Vertical-Nanowire Tunnel-FETs. *IEEE Transactions on Device and Materials Reliability*, **2017**, 17, 253-258	1.6	2
121	Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. *Progress in Photovoltaics: Research and Applications*, **2017**, 25, 452-469	6.8	27
120	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. *IEEE Transactions on Electron Devices*, **2017**, 64, 2736-2743	2.9	39
119	Impact of AlN layer sandwiched between the GaN and the Al2O3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs. *Microelectronic Engineering*, **2017**, 178, 42-47	2.5	18

118	On recoverable behavior of PBTI in AlGaN/GaN MOS-HEMT. *Solid-State Electronics*, **2017**, 132, 49-56	1.7	20
117	Modelling doping design in nanowire tunnel-FETs based on group-IV semiconductors. *Materials Science in Semiconductor Processing*, **2017**, 62, 201-204	4.3	5
116	Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. *IEEE Nanotechnology Magazine*, **2017**, 16, 160-168	2.6	22
115	Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. *Solar Energy*, **2017**, 155, 1443-1450	6.8	1
114	A variation-aware simulation framework for hybrid CMOS/spintronic circuits **2017**,		3
113	Impact of voltage scaling on STT-MRAMs through a variability-aware simulation framework **2017**,		4
112	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits. *Solid-State Electronics*, **2017**, 128, 37-42	1.7	12
111	Tuning the switching behavior of conductive-bridge resistive memory by the modulation of the cation-supplier alloys. *Microelectronic Engineering*, **2017**, 167, 47-51	2.5	8
110	A physical unclonable function based on a 2-transistor subthreshold voltage divider. *International Journal of Circuit Theory and Applications*, **2017**, 45, 260-273	2	7
109	Low energy/delay overhead level shifter for wide-range voltage conversion. *International Journal of Circuit Theory and Applications*, **2017**, 45, 1637-1646	2	3
108	A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. *IEEE Transactions on Electron Devices*, **2017**, 64, 4346-4353	2.9	26
107	Electrical Characterization of the Influence of the Annealing Energy Density on Carrier Lifetimes in Germanium. *ECS Journal of Solid State Science and Technology*, **2016**, 5, P3013-P3017	2	2
106	Numerical simulation of the impact of design parameters on the performance of back-contact back-junction solar cell. *Journal of Computational Electronics*, **2016**, 15, 260-268	1.8	12
105	Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. *IEEE Transactions on Electron Devices*, **2016**, 63, 2749-2756	2.9	33
104	Structural and Electrical Investigation of MoS2Thin Films Formed by Thermal Assisted Conversion of Mo Metal. *ECS Journal of Solid State Science and Technology*, **2016**, 5, Q3016-Q3020	2	4
103	Back-gated Nb-doped MoS2 junctionless field-effect-transistors. *AIP Advances*, **2016**, 6, 025323	1.5	15
102	Low Frequency Noise and Gate Bias Instability in Normally OFF AlGaN/GaN HEMTs. *IEEE Transactions on Electron Devices*, **2016**, 63, 2219-2222	2.9	16
101	Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells. *Journal of Computational Electronics*, **2016**, 15, 1498-1504	1.8	1

100	Implications of the Incremental Pulse and Verify Algorithm on the Forming and Switching Distributions in RERAM Arrays. *IEEE Transactions on Device and Materials Reliability*, **2016**, 16, 413-418	1.6	7
99	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells. *IEEE Journal of the Electron Devices Society*, **2015**, 3, 223-232	2.3	53
98	A Defect-Centric perspective on channel hot carrier variability in nMOSFETs. *Microelectronic Engineering*, **2015**, 147, 72-74	2.5	4
97	Resistive switching characteristics of integrated polycrystalline hafnium oxide based one transistor and one resistor devices fabricated by atomic vapor deposition methods. *Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics*, **2015**, 33, 052204	1.3	16
96	Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. *IEEE Transactions on Electron Devices*, **2015**, 62, 3973-3979	2.9	47
95	Gate-level body biasing for subthreshold logic circuits: analytical modeling and design guidelines. *International Journal of Circuit Theory and Applications*, **2015**, 43, 1523-1540	2	7
94	Understanding the Optimization of the Emitter Coverage in BC-BJ Solar Cells. *Energy Procedia*, **2015**, 77, 149-152	2.3	2
93	A sub-1 V nanopower temperature-compensated sub-threshold CMOS voltage reference with 0.065%/V line sensitivity. *International Journal of Circuit Theory and Applications*, **2015**, 43, 421-426	2	4
92	Measurements and Simulations on the Mechanisms of Efficiency Losses in HIT Solar Cells. *International Journal of Photoenergy*, **2015**, 2015, 1-7	2.1	1
91	A Sub- ${boldsymbol kT}/boldsymbol q$ Voltage Reference Operating at 150 mV. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1547-1551	2.6	39
90	A picopower temperature-compensated, subthreshold CMOS voltage reference. *International Journal of Circuit Theory and Applications*, **2014**, 42, 1306-1318	2	14
89	Border Traps in InGaAs nMOSFETs Assessed by Low-Frequency Noise. *IEEE Electron Device Letters*, **2014**, 35, 720-722	4.4	9
88	Analysis of the impact of rear side geometry on performance of back-contact back-junction solar cells **2014**,		3
87	Defect-Centric Distribution of Channel Hot Carrier Degradation in Nano-MOSFETs. *IEEE Electron Device Letters*, **2014**, 35, 1167-1169	4.4	12
86	Analysis of the Impact of Doping Levels on Performance of back Contact-Back Junction Solar Cells. *Energy Procedia*, **2014**, 55, 128-132	2.3	9
85	Analysis of TFET based 6T SRAM cells implemented with state of the art silicon nanowires **2014**,		4
84	Impact of the Substrate Orientation on CHC Reliability in n-FinFETs: Separation of the Various Contributions. *IEEE Transactions on Device and Materials Reliability*, **2014**, 14, 52-56	1.6	14
83	Low-frequency noise assessment of border traps in Al2O3 capped DRAM peripheral MOSFETs. *Semiconductor Science and Technology*, **2014**, 29, 115015	1.8	13

82	Design of a 75-nW, 0.5-V subthreshold complementary metal□oxide□semiconductor operational amplifier. *International Journal of Circuit Theory and Applications*, **2014**, 42, 967-977	2	41
81	. *IEEE Journal of Photovoltaics*, **2013**, 3, 1215-1221	3.7	11
80	DC and low-frequency noise behavior of the conductive filament in bipolar HfO2-based resistive random access memory. *Microelectronic Engineering*, **2013**, 107, 1-5	2.5	12
79	A Comparative Study of MWT Architectures by Means of Numerical Simulations. *Energy Procedia*, **2013**, 38, 131-136	2.3	1
78	Impact of High-Mobility Materials on the Performance of Near- and Sub-Threshold CMOS Logic Circuits. *IEEE Transactions on Electron Devices*, **2013**, 60, 972-977	2.9	7
77	Forward to the Special Section on □eliability of High-Mobility Channel Materials□*IEEE Transactions on Device and Materials Reliability*, **2013**, 13, 428-428	1.6	
76	Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2012**, 59, 439-442	2.5	23
75	A Methodology to Account for the Finger Non-Uniformity in Photovoltaic Solar Cell. *Energy Procedia*, **2012**, 27, 191-196	2.3	9
74	Buried Silicon-Germanium pMOSFETs: Experimental Analysis in VLSI Logic Circuits Under Aggressive Voltage Scaling. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 1487-1495	2.6	6
73	BTI reliability of ultra-thin EOT MOSFETs for sub-threshold logic. *Microelectronics Reliability*, **2012**, 52, 1932-1935	1.2	9
72	A methodology to account for the finger interruptions in solar cell performance. *Microelectronics Reliability*, **2012**, 52, 2500-2503	1.2	7
71	Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region. *IEEE Transactions on Electron Devices*, **2012**, 59, 2093-2099	2.9	16
70	Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates. *Journal of Applied Physics*, **2012**, 111, 124104	2.5	16
69	Experimental analysis of buried SiGe pMOSFETs from the perspective of aggressive voltage scaling **2011**,		1
68	A Backscattering Model Incorporating the Effective Carrier Temperature in Nano-MOSFET. *IEEE Electron Device Letters*, **2011**, 32, 853-855	4.4	4
67	. *IEEE Journal of Solid-State Circuits*, **2011**, 46, 465-474	5.5	164
66	. *IEEE Transactions on Electron Devices*, **2011**, 58, 691-697	2.9	8
65	. *IEEE Transactions on Electron Devices*, **2011**, 58, 2347-2353	2.9	40

64	Criticisms on and comparison of experimental channel backscattering extraction methods. *Microelectronic Engineering*, **2011**, 88, 76-81	2.5	4
63	Si1-xGex-Channel PFETs: Scalability, Layout Considerations and Compatibility with Other Stress Techniques. *ECS Transactions*, **2011**, 35, 493-503	1	7
62	Structural and Electrical Analysis of Thin Interface Control Layers of MgO or Al2O3 Deposited by Atomic Layer Deposition and Incorporated at the High-k/III-V Interface of MO2/InxGa1-xAs (M = Hf|Zr, x = 0|0.53) Gate Stacks. *ECS Transactions*, **2010**, 33, 69-82	1	7
61	. *IEEE Transactions on Nuclear Science*, **2010**, 57, 2309-2317	1.7	11
60	Bipolar Mode Operation and Scalability of Double-Gate Capacitorless 1T-DRAM Cells. *IEEE Transactions on Electron Devices*, **2010**, 57, 1743-1750	2.9	27
59	Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs. *IEEE Transactions on Electron Devices*, **2010**, 57, 2132-2137	2.9	14
58	FinFET Mismatch in Subthreshold Region: Theory and Experiments. *IEEE Transactions on Electron Devices*, **2010**, 57, 2848-2856	2.9	18
57	Implications of fin width scaling on variability and reliability of high-k metal gate FinFETs. *Microelectronic Engineering*, **2010**, 87, 1963-1967	2.5	12
56	Multiple gate NVM cells with improved Fowler Nordheim tunneling program and erase performances. *Solid-State Electronics*, **2010**, 54, 1319-1325	1.7	1
55	Matching Performance of FinFET Devices With Fin Widths Down to 10 nm. *IEEE Electron Device Letters*, **2009**, 30, 1374-1376	4.4	20
54	The Role of the Interfaces in the 1/f Noise of MOSFETs with High-k Gate Stacks. *ECS Transactions*, **2009**, 19, 87-99	1	5
53	. *IEEE Transactions on Electron Devices*, **2009**, 56, 1063-1069	2.9	15
52	Cross-correlation-based trans-impedance amplifier for current noise measurements. *International Journal of Circuit Theory and Applications*, **2009**, 37, 781-792	2	12
51	$1/f$ Noise in Drain and Gate Current of MOSFETs With High-k Gate Stacks. *IEEE Transactions on Device and Materials Reliability*, **2009**, 9, 180-189	1.6	86
50	Full Model and Characterization of Noise in Operational Amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2009**, 56, 97-102	3.9	7
49	On the Temperature and Field Dependence of Trap-Assisted Tunneling Current in Ge $hbox{p}^{+}hbox{n}$ Junctions. *IEEE Electron Device Letters*, **2009**, 30, 562-564	4.4	41
48	Detection and Classification of Single-Electron Jumps in Si Nanocrystal Memories. *IEEE Transactions on Instrumentation and Measurement*, **2008**, 57, 364-368	5.2	3
47	Impact of Si-thickness on interface and device properties for Si-passivated Ge pMOSFETs **2008**,		15

46	On the Impact of Defects Close to the Gate Electrode on the Low-Frequency $hbox{1}/f$ Noise. *IEEE Electron Device Letters*, **2008**, 29, 1056-1058	4.4	7
45	On the dc and noise properties of the gate current in epitaxial Ge p-channel metal oxide semiconductor field effect transistors with TiNTaNHfO2SiO2 gate stack. *Applied Physics Letters*, **2008**, 92, 163508	3.4	12
44	Electron transport through electrically induced nanoconstrictions in HfSiON gate stacks. *Applied Physics Letters*, **2008**, 92, 253505	3.4	4
43	Performance of current mirror with high-k gate dielectrics. *Microelectronic Engineering*, **2008**, 85, 284-288	2.5	4
42	Gate voltage and geometry dependence of the series resistance and of the carrier mobility in FinFET devices. *Microelectronic Engineering*, **2008**, 85, 1728-1731	2.5	13
41	Impact strain engineering on gate stack quality and reliability. *Solid-State Electronics*, **2008**, 52, 1115-1126	1.7	56
40	Impact of the variable output resistance on the transient response of LC transmission line CMOS buffers and its model. *Microwave and Optical Technology Letters*, **2007**, 49, 1504-1509	1.2	
39	Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias. *Microelectronic Engineering*, **2007**, 84, 1947-1950	2.5	2
38	Comparison of stressed Poly-Si and TiN gated Hf-based NMOSFETs characteristics, modeling and their impact on circuits performance. *Microelectronic Engineering*, **2007**, 84, 2113-2116	2.5	
37	Low frequency noise in nMOSFETs with subnanometer EOT hafnium-based gate dielectrics. *Microelectronics Reliability*, **2007**, 47, 2109-2113	1.2	2
36	A New Circuit Topology for the Realization of Very Low-Noise Wide-Bandwidth Transimpedance Amplifier. *IEEE Transactions on Instrumentation and Measurement*, **2007**, 56, 1626-1631	5.2	18
35	Performance and Reliability of Strained-Silicon nMOSFETs With SiN Cap Layer. *IEEE Transactions on Electron Devices*, **2007**, 54, 78-82	2.9	12
34	Modeling of Tunnelling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters. *IEEE Transactions on Electron Devices*, **2007**, 54, 83-89	2.9	36
33	Interfacial layer quality effects on low-frequency noise (1/f) in p-MOSFETs with advanced gate stacks. *Microelectronics Reliability*, **2007**, 47, 501-504	1.2	3
32	Single-Electron Program/Erase Tunnel Events in Nanocrystal Memories. *IEEE Nanotechnology Magazine*, **2007**, 6, 35-42	2.6	8
31	Two-channel amplifier for high-sensitivity voltage noise measurements. *Conference Record - IEEE Instrumentation and Measurement Technology Conference*, **2007**,		3
30	Comparative study of drain and gate low-frequency noise in nMOSFETs with hafnium-based gate dielectrics. *IEEE Transactions on Electron Devices*, **2006**, 53, 823-828	2.9	72
29	Reliability Comparison of Triple-Gate Versus Planar SOI FETs. *IEEE Transactions on Electron Devices*, **2006**, 53, 2351-2357	2.9	43

28	How to enlarge the bandwidth without increasing the noise in OP-AMP-based transimpedance amplifier. *IEEE Transactions on Instrumentation and Measurement*, **2006**, 55, 814-819	5.2	24
27	Three-channel amplifier for high-sensitivity voltage noise measurements. *Review of Scientific Instruments*, **2006**, 77, 095104	1.7	6
26	Low-frequency (1/f) noise behavior of locally stressed HfO/sub 2//TiN gate-stack pMOSFETs. *IEEE Electron Device Letters*, **2006**, 27, 508-510	4.4	24
25	Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks. *IEEE Electron Device Letters*, **2006**, 27, 688-691	4.4	45
24	Enhanced sensitivity cross-correlation method for voltage noise measurements. *IEEE Transactions on Instrumentation and Measurement*, **2006**, 55, 1143-1147	5.2	13
23	A novel methodology for sensing the breakdown location and its application to the reliability study of ultrathin Hf-silicate gate dielectrics. *IEEE Transactions on Electron Devices*, **2005**, 52, 1759-1765	2.9	12
22	Positive Bias Temperature Instability in nMOSFETs with ultra-thin Hf-silicate gate dielectrics. *Microelectronic Engineering*, **2005**, 80, 130-133	2.5	32
21	Room-temperature single-electron effects in silicon nanocrystal memories. *Applied Physics Letters*, **2005**, 87, 182106	3.4	18
20	Modeling pFET currents after soft breakdown at different gate locations. *Microelectronic Engineering*, **2004**, 72, 125-129	2.5	
19	Theory and experiment of suppressed shot noise in 'stress-induced leakage currents. *IEEE Transactions on Electron Devices*, **2003**, 50, 1363-1369	2.9	21
18	Very low-noise, high-accuracy programmable voltage reference. *IEEE Transactions on Instrumentation and Measurement*, **2003**, 52, 1251-1254	5.2	18
17	Micro-prober for wafer-level low-noise measurements in MOS devices. *IEEE Transactions on Instrumentation and Measurement*, **2003**, 52, 1533-1536	5.2	12
16	A comparative study of the oxide breakdown in short-channel nMOSFETs and pMOSFETs stressed in inversion and in accumulation regimes. *IEEE Transactions on Device and Materials Reliability*, **2003**, 3, 8-13	1.6	12
15	New insights into the relation between channel hot carrier degradation and oxide breakdown short channel nMOSFETs. *IEEE Electron Device Letters*, **2003**, 24, 278-280	4.4	12
14	Low frequency current noise in unstressed/stressed thin oxide metal-oxide-semiconductor capacitors. *Solid-State Electronics*, **2002**, 46, 1807-1813	1.7	5
13	On the role of interface states in low-voltage leakage currents of metal□oxide□semiconductor structures. *Applied Physics Letters*, **2002**, 80, 4597-4599	3.4	24
12	Current noise at the oxide hard-breakdown. *Microelectronic Engineering*, **2001**, 59, 43-47	2.5	4
11	Characterization of soft breakdown in thin oxide NMOSFETs based on the analysis of the substrate current. *IEEE Transactions on Electron Devices*, **2001**, 48, 1109-1113	2.9	10

10	Reduction of thermal damage in ultrathin gate oxides after intrinsic dielectric breakdown. *Applied Physics Letters*, **2001**, 79, 1522-1524	3.4	15
9	Shot noise partial suppression in the SILO regime. *Microelectronics Reliability*, **2000**, 40, 1605-1608	1.2	8
8	Suppressed shot noise in trap-assisted tunneling of metal–oxide–semiconductor capacitors. *Applied Physics Letters*, **2000**, 77, 2876-2878	3.4	18
7	Pre-breakdown in thin SiO2 films. *IEEE Electron Device Letters*, **2000**, 21, 319-321	4.4	17
6	Investigation and Comparison of the Noise in the Gate and Substrate Current after Soft-Breakdown. *Japanese Journal of Applied Physics*, **1999**, 38, 2219-2222	1.4	7
5	Soft breakdown of gate oxides in metal–SiO2–Si capacitors under stress with hot electrons. *Applied Physics Letters*, **1999**, 75, 1161-1163	3.4	19
4	Transients during pre-breakdown and hard breakdown of thin gate oxides in metal–SiO2–Si capacitors. *Materials Science in Semiconductor Processing*, **1999**, 2, 359-367	4.3	2
3	Degradation and hard breakdown transient of thin gate oxides in metal–SiO2–Si capacitors: Dependence on oxide thickness. *Journal of Applied Physics*, **1999**, 86, 6382-6391	2.5	74
2	On the properties of the gate and substrate current after soft breakdown in ultrathin oxide layers. *IEEE Transactions on Electron Devices*, **1998**, 45, 2329-2334	2.9	78
1	Electrical and thermal transient during dielectric breakdown of thin oxides in metal-SiO2-silicon capacitors. *Journal of Applied Physics*, **1998**, 84, 472-479	2.5	54