Felice Crupi

List of Publications by Year
in descending order

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168	3,217	28	47
papers	citations	h-index	g-index
		186209	214721

168	168	168	2387
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference. IEEE Journal of Solid-State Circuits, 2011, 46, 465-474.	3.5	244
2	$1/f$ Noise in Drain and Gate Current of MOSFETs With High-k Gate Stacks. IEEE Transactions on Device and Materials Reliability, 2009, 9, 180-189.	1.5	107
3	Comparative study of drain and gate low-frequency noise in nMOSFETs with hafnium-based gate dielectrics. IEEE Transactions on Electron Devices, 2006, 53, 823-828.	1.6	97
4	On the properties of the gate and substrate current after soft breakdown in ultrathin oxide layers. IEEE Transactions on Electron Devices, 1998, 45, 2329-2334.	1.6	94
5	Degradation and hard breakdown transient of thin gate oxides in metalâ€“SiO2â€“Si capacitors: Dependence on oxide thickness. Journal of Applied Physics, 1999, 86, 6382-6391.	1.1	80
6	Design of a 75â€nW, 0.5â€V subthreshold complementary metalâ€“oxideâ€“semiconductor operational amplifier. International Journal of Circuit Theory and Applications, 2014, 42, 967-977.	1.3	75
7	Impact strain engineering on gate stack quality and reliability. Solid-State Electronics, 2008, 52, 1115-1126.	0.8	69
8	Impact of TFET Unidirectionality and Ambipolarity on the Performance of 6T SRAM Cells. IEEE Journal of the Electron Devices Society, 2015, 3, 223-232.	1.2	68
9	An Ultralow-Voltage Energy-Efficient Level Shifter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 61-65.	2.2	67
10	A Sub-<inline-formula> <tex-math notation="LaTeX">${oldsymbol kT}/oldsymbol q$ </tex-math></inline-formula> Voltage Reference Operating at 150 mV. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1547-1551.	2.1	64
11	Electrical and thermal transient during dielectric breakdown of thin oxides in metal-SiO2-silicon capacitors. Journal of Applied Physics, 1998, 84, 472-479.	1.1	62
12	Digital and analog TFET circuits: Design and benchmark. Solid-State Electronics, 2018, 146, 50-65.	0.8	60
13	Mixed Tunnel-FET/MOSFET Level Shifters: A New Proposal to Extend the Tunnel-FET Application Domain. IEEE Transactions on Electron Devices, 2015, 62, 3973-3979.	1.6	59
14	Understanding the Potential and Limitations of Tunnel FETs for Low-Voltage Analog/Mixed-Signal Circuits. IEEE Transactions on Electron Devices, 2017, 64, 2736-2743.	1.6	57
15	Impact of the interfacial layer on the low-frequency noise (1/f) behavior of MOSFETs with advanced gate stacks. IEEE Electron Device Letters, 2006, 27, 688-691.	2.2	54
16	Impact of Hot Carriers on nMOSFET Variability in 45- and 65-nm CMOS Technologies. IEEE Transactions on Electron Devices, 2011, 58, 2347-2353.	1.6	50
17	On the Temperature and Field Dependence of Trap-Assisted Tunneling Current in Ge $hbox{p}^{+}hbox{n}$ Junctions. IEEE Electron Device Letters, 2009, 30, 562-564.	2.2	49
18	Reliability Comparison of Triple-Gate Versus Planar SOI FETs. IEEE Transactions on Electron Devices, 2006, 53, 2351-2357.	1.6	47

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19	Assessment of InAs/AlGaSb Tunnel-FET Virtual Technology Platform for Low-Power Digital Circuits. IEEE Transactions on Electron Devices, 2016, 63, 2749-2756.	1.6	44
20	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1086-1095.	3.5	41
21	Modeling of Tunnelling Currents in Hf-Based Gate Stacks as a Function of Temperature and Extraction of Material Parameters. IEEE Transactions on Electron Devices, 2007, 54, 83-89.	1.6	40
22	A Compact Model with Spin-Polarization Asymmetry for Nanoscaled Perpendicular MTJs. IEEE Transactions on Electron Devices, 2017, 64, 4346-4353.	1.6	40
23	Positive Bias Temperature Instability in nMOSFETs with ultra-thin Hf-silicate gate dielectrics. Microelectronic Engineering, 2005, 80, 130-133.	1.1	36
24	Bipolar Mode Operation and Scalability of Double-Gate Capacitorless 1T-DRAM Cells. IEEE Transactions on Electron Devices, 2010, 57, 1743-1750.	1.6	33
25	Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 439-442.	2.2	33
26	Opto-electrical modelling and optimization study of a novel IBC c-Si solar cell. Progress in Photovoltaics: Research and Applications, 2017, 25, 452-469.	4.4	33
27	How to Enlarge the Bandwidth Without Increasing the Noise in OP-AMP-Based Transimpedance Amplifier. IEEE Transactions on Instrumentation and Measurement, 2006, 55, 814-819.	2.4	29
28	Matching Performance of FinFET Devices With Fin Widths Down to 10 nm. IEEE Electron Device Letters, 2009, 30, 1374-1376.	2.2	28
29	Variability-Aware Analysis of Hybrid MTJ/CMOS Circuits by a Micromagnetic-Based Simulation Framework. IEEE Nanotechnology Magazine, 2017, 16, 160-168.	1.1	28
30	Low-frequency (1/f) noise behavior of locally stressed HfO/sub 2//TiN gate-stack pMOSFETs. IEEE Electron Device Letters, 2006, 27, 508-510.	2.2	27
31	Numerical simulations of hole carrier selective contacts in p-type c-Si solar cells. Solar Energy Materials and Solar Cells, 2019, 200, 109937.	3.0	27
32	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. IEEE Journal of Solid-State Circuits, 2021, 56, 3134-3144.	3.5	27
33	On the role of interface states in low-voltage leakage currents of metalâ€“oxideâ€“semiconductor structures. Applied Physics Letters, 2002, 80, 4597-4599.	1.5	26
34	Theory and experiment of suppressed shot noise in stress-induced leakage currents. IEEE Transactions on Electron Devices, 2003, 50, 1363-1369.	1.6	26
35	Compact Modeling of Perpendicular STT-MTJs With Double Reference Layers. IEEE Nanotechnology Magazine, 2019, 18, 1063-1070.	1.1	25
36	Room-temperature single-electron effects in silicon nanocrystal memories. Applied Physics Letters, 2005, 87, 182106.	1.5	24

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37	A New Circuit Topology for the Realization of Very Low-Noise Wide-Bandwidth Transimpedance Amplifier. IEEE Transactions on Instrumentation and Measurement, 2007, 56, 1626-1631.	2.4	24
38	On recoverable behavior of PBTI in AlGaN/GaN MOS-HEMT. Solid-State Electronics, 2017, 132, 49-56.	0.8	24
39	Reliability Improvements in AlGaN/GaN Schottky Barrier Diodes With a Gated Edge Termination. IEEE Transactions on Electron Devices, 2018, 65, 1765-1770.	1.6	24
40	Assessment of STT-MRAM performance at nanoscaled technology nodes using a device-to-memory simulation framework. Microelectronic Engineering, 2019, 215, 111009.	1.1	24
41	Soft breakdown of gate oxides in metalâ€“SiO2â€“Si capacitors under stress with hot electrons. Applied Physics Letters, 1999, 75, 1161-1163.	1.5	23
42	FinFET Mismatch in Subthreshold Region: Theory and Experiments. IEEE Transactions on Electron Devices, 2010, 57, 2848-2856.	1.6	23
43	Low Frequency Noise and Gate Bias Instability in Normally OFF AlGaN/GaN HEMTs. IEEE Transactions on Electron Devices, 2016, 63, 2219-2222.	1.6	23
44	Pre-breakdown in thin SiO2 films. IEEE Electron Device Letters, 2000, 21, 319-321.	2.2	22
45	Impact of AlN layer sandwiched between the GaN and the Al2O3 layers on the performance and reliability of recessed AlGaN/GaN MOS-HEMTs. Microelectronic Engineering, 2017, 178, 42-47.	1.1	22
46	Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework. The Integration VLSI Journal, 2020, 71, 56-69.	1.3	22
47	Suppressed shot noise in trap-assisted tunneling of metalâ€“oxideâ€“semiconductor capacitors. Applied Physics Letters, 2000, 77, 2876-2878.	1.5	21
48	Very low-noise, high-accuracy programmable voltage reference. IEEE Transactions on Instrumentation and Measurement, 2003, 52, 1251-1254.	2.4	21
49	Understanding and Optimization of Hot-Carrier Reliability in Germanium-on-Silicon pMOSFETs. IEEE Transactions on Electron Devices, 2009, 56, 1063-1069.	1.6	21
50	A picopower temperatureâ€compensated, subthreshold CMOS voltage reference. International Journal of Circuit Theory and Applications, 2014, 42, 1306-1318.	1.3	21
51	Exploiting STT-MRAMs for Cryogenic Non-Volatile Cache Applications. IEEE Nanotechnology Magazine, 2021, 20, 123-128.	1.1	21
52	Characterization and Modeling of Hot Carrier-Induced Variability in Subthreshold Region. IEEE Transactions on Electron Devices, 2012, 59, 2093-2099.	1.6	20
53	Back-gated Nb-doped MoS2 junctionless field-effect-transistors. AIP Advances, 2016, 6, .	0.6	20
54	Enhanced Sensitivity Cross-Correlation Method for Voltage Noise Measurements. IEEE Transactions on Instrumentation and Measurement, 2006, 55, 1143-1147.	2.4	19

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55	Observation of peripheral charge induced low frequency capacitance-voltage behaviour in metal-oxide-semiconductor capacitors on Si and GaAs substrates. Journal of Applied Physics, 2012, 111, .	1.1	19
56	Defect-Centric Distribution of Channel Hot Carrier Degradation in Nano-MOSFETs. IEEE Electron Device Letters, 2014, 35, 1167-1169.	2.2	19
57	Impact of the Substrate Orientation on CHC Reliability in n-FinFETsâ€"Separation of the Various Contributions. IEEE Transactions on Device and Materials Reliability, 2014, 14, 52-56.	1.5	19
58	Diagnosis of phosphorus monolayer doping in silicon based on nanowire electrical characterisation. Journal of Applied Physics, 2018, 123, 125701.	1.1	19
59	New insights into the relation between channel hot carrier degradation and oxide breakdown short channel nMOSFETs. IEEE Electron Device Letters, 2003, 24, 278-280.	2.2	17
60	Performance and Reliability of Strained-Silicon nMOSFETs With SiN Cap Layer. IEEE Transactions on Electron Devices, 2007, 54, 78-82.	1.6	17
61	Gate voltage and geometry dependence of the series resistance and of the carrier mobility in FinFET devices. Microelectronic Engineering, 2008, 85, 1728-1731.	1.1	17
62	On the dc and noise properties of the gate current in epitaxial Ge p-channel metal oxide semiconductor field effect transistors with TiNâˆ•TaNâˆ•HfO2âˆ•SiO2 gate stack. Applied Physics Letters, 2008, 92, .	1.5	17
63	Resistive switching characteristics of integrated polycrystalline hafnium oxide based one transistor and one resistor devices fabricated by atomic vapor deposition methods. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2015, 33, 052204.	0.6	17
64	Benchmarks of a III-V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits. Solid-State Electronics, 2017, 128, 37-42.	0.8	17
65	Impact of Si-thickness on interface and device properties for Si-passivated Ge pMOSFETs. , 2008, , .		16
66	Barrier Lowering and Backscattering Extraction in Short-Channel MOSFETs. IEEE Transactions on Electron Devices, 2010, 57, 2132-2137.	1.6	16
67	Implications of fin width scaling on variability and reliability of high-k metal gate FinFETs. Microelectronic Engineering, 2010, 87, 1963-1967.	1.1	16
68	A physical unclonable function based on a 2â€transistor subthreshold voltage divider. International Journal of Circuit Theory and Applications, 2017, 45, 260-273.	1.3	16
69	A portable class of 3â€transistor current references with lowâ€power subâ€0.5Â<scp>V</scp> operation. International Journal of Circuit Theory and Applications, 2018, 46, 779-795.	1.3	16
70	Simulation Analysis of DMTJ-Based STT-MRAM Operating at Cryogenic Temperatures. IEEE Transactions on Magnetics, 2021, 57, 1-6.	1.2	16
71	Reduction of thermal damage in ultrathin gate oxides after intrinsic dielectric breakdown. Applied Physics Letters, 2001, 79, 1522-1524.	1.5	15
72	Micro-prober for wafer-level low-noise measurements in MOS devices. IEEE Transactions on Instrumentation and Measurement, 2003, 52, 1533-1536.	2.4	15

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73	Crossâ€correlationâ€based transâ€impedance amplifier for current noise measurements. International Journal of Circuit Theory and Applications, 2009, 37, 781-792.	1.3	15
74	A comparative study of the oxide breakdown in short-channel nmosfets and pmosfets stressed in inversion and in accumulation regimes. IEEE Transactions on Device and Materials Reliability, 2003, 3, 8-13.	1.5	14
75	Full Model and Characterization of Noise in Operational Amplifier. IEEE Transactions on Circuits and Systems I: Regular Papers, 2009, 56, 97-102.	3.5	14
76	Radiation Tolerance of NROM Embedded Products. IEEE Transactions on Nuclear Science, 2010, 57, 2309-2317.	1.2	14
77	DC and low-frequency noise behavior of the conductive filament in bipolar HfO2-based resistive random access memory. Microelectronic Engineering, 2013, 107, 1-5.	1.1	14
78	Low-frequency noise assessment of border traps in Al₂O₃ capped DRAM peripheral MOSFETs. Semiconductor Science and Technology, 2014, 29, 115015.	1.0	14
79	Numerical simulation of the impact of design parameters on the performance of back-contact back-junction solar cell. Journal of Computational Electronics, 2016, 15, 260-268.	1.3	14
80	A Novel Methodology for Sensing the Breakdown Location and Its Application to the Reliability Study of Ultrathin Hf-Silicate Gate Dielectrics. IEEE Transactions on Electron Devices, 2005, 52, 1759-1765.	1.6	13
81	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1393-1397.	2.2	13
82	Characterization of soft breakdown in thin oxide NMOSFETs based on the analysis of the substrate current. IEEE Transactions on Electron Devices, 2001, 48, 1109-1113.	1.6	12
83	A Methodology to Account for the Finger Non-Uniformity in Photovoltaic Solar Cell. Energy Procedia, 2012, 27, 191-196.	1.8	12
84	Numerical Simulation and Modeling of Resistive and Recombination Losses in MWT Solar Cells. IEEE Journal of Photovoltaics, 2013, 3, 1215-1221.	1.5	12
85	A 0.05 mmÂ², 350 mV, 14 nW Fully-Integrated Temperature Sensor in 180-nm CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 749-753.	2.2	12
86	Relaxing non-volatility for energy-efficient DMTJ based cryogenic STT-MRAM. Solid-State Electronics, 2021, 184, 108090.	0.8	12
87	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3038-3042.	2.2	11
88	Static CMOS Physically Unclonable Function Based on 4T Voltage Divider With 0.6%â€“1.5% Bit Instability at 0.4â€“1.8 V Operation in 180 nm. IEEE Journal of Solid-State Circuits, 2022, 57, 2509-2520.	3.5	11
89	Shot noise partial suppression in the SILO regime. Microelectronics Reliability, 2000, 40, 1605-1608.	0.9	10
90	Analysis of the Impact of Doping Levels on Performance of back Contact-Back Junction Solar Cells. Energy Procedia, 2014, 55, 128-132.	1.8	10

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91	Border Traps in InGaAs nMOSFETs Assessed by Low-Frequency Noise. IEEE Electron Device Letters, 2014, 35, 720-722.	2.2	10
92	Single-Electron Program/Erase Tunnel Events in Nanocrystal Memories. IEEE Nanotechnology Magazine, 2007, 6, 35-42.	1.1	9
93	Structural and Electrical Analysis of Thin Interface Control Layers of MgO or Al₂O₃ Deposited by Atomic Layer Deposition and Incorporated at the High-k/III-V Interface of MO₂/In_xGa_{1-x}As (M = Hf | Zr, x = 0 | 0.53) Gate Stacks. ECS Transactions, 2010, 33, 69-82.	0.3	9
94	A Microscopically Accurate Model of Partially Ballistic NanoMOSFETs in Saturation Based on Channel Backscattering. IEEE Transactions on Electron Devices, 2011, 58, 691-697.	1.6	9
95	BTI reliability of ultra-thin EOT MOSFETs for sub-threshold logic. Microelectronics Reliability, 2012, 52, 1932-1935.	0.9	9
96	A methodology to account for the finger interruptions in solar cell performance. Microelectronics Reliability, 2012, 52, 2500-2503.	0.9	9
97	Impact of High-Mobility Materials on the Performance of Near- and Sub-Threshold CMOS Logic Circuits. IEEE Transactions on Electron Devices, 2013, 60, 972-977.	1.6	9
98	STT-MTJ Based Smart Implication for Energy-Efficient Logic-in-Memory Computing. Solid-State Electronics, 2021, 184, 108065.	0.8	9
99	Investigation and Comparison of the Noise in the Gate and Substrate Current after Soft-Breakdown. Japanese Journal of Applied Physics, 1999, 38, 2219-2222.	0.8	8
100	Three-channel amplifier for high-sensitivity voltage noise measurements. Review of Scientific Instruments, 2006, 77, 095104.	0.6	8
101	Si1-xGex-Channel PFETs: Scalability, Layout Considerations and Compatibility with Other Stress Techniques. ECS Transactions, 2011, 35, 493-503.	0.3	8
102	Buried Silicon-Germanium pMOSFETs: Experimental Analysis in VLSI Logic Circuits Under Aggressive Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 1487-1495.	2.1	8
103	Gateâ€level body biasing for subthreshold logic circuits: analytical modeling and design guidelines. International Journal of Circuit Theory and Applications, 2015, 43, 1523-1540.	1.3	8
104	Tuning the switching behavior of conductive-bridge resistive memory by the modulation of the cation-supplier alloys. Microelectronic Engineering, 2017, 167, 47-51.	1.1	8
105	Low frequency current noise in unstressed/stressed thin oxide metal-oxide-semiconductor capacitors. Solid-State Electronics, 2002, 46, 1807-1813.	0.8	7
106	On the Impact of Defects Close to the Gate Electrode on the Low-Frequency $hbox{1}/f$ Noise. IEEE Electron Device Letters, 2008, 29, 1056-1058.	2.2	7
107	Implications of the Incremental Pulse and Verify Algorithm on the Forming and Switching Distributions in RERAM Arrays. IEEE Transactions on Device and Materials Reliability, 2016, 16, 413-418.	1.5	7
108	Modelling doping design in nanowire tunnel-FETs based on group-IV semiconductors. Materials Science in Semiconductor Processing, 2017, 62, 201-204.	1.9	7

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109	BTI saturation and universal relaxation in SiC power MOSFETs. Microelectronics Reliability, 2020, 109, 113642.	0.9	7
110	Reliability Assessment of AlGaN/GaN Schottky Barrier Diodes Under ON-State Stress. IEEE Transactions on Device and Materials Reliability, 2020, 20, 167-171.	1.5	7
111	The Role of the Interfaces in the 1/f Noise of MOSFETs with High-k Gate Stacks. ECS Transactions, 2009, 19, 87-99.	0.3	6
112	Analysis of TFET based 6T SRAM cells implemented with state of the art silicon nanowires. , 2014, , .		6
113	A Defect-Centric perspective on channel hot carrier variability in nMOSFETs. Microelectronic Engineering, 2015, 147, 72-74.	1.1	6
114	Structural and Electrical Investigation of MoS₂Thin Films Formed by Thermal Assisted Conversion of Mo Metal. ECS Journal of Solid State Science and Technology, 2016, 5, Q3016-Q3020.	0.9	6
115	Impact of voltage scaling on STT-MRAMs through a variability-aware simulation framework. , 2017, , .		6
116	Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs. , 2019, , .		6
117	A Low-Voltage, Low-Power Reconfigurable Current-Mode Softmax Circuit for Analog Neural Networks. Electronics (Switzerland), 2021, 10, 1004.	1.8	6
118	Current noise at the oxide hard-breakdown. Microelectronic Engineering, 2001, 59, 43-47.	1.1	5
119	A Backscattering Model Incorporating the Effective Carrier Temperature in Nano-MOSFET. IEEE Electron Device Letters, 2011, 32, 853-855.	2.2	5
120	A subâ€1â€‰V nanopower temperatureâ€compensated subâ€threshold CMOS voltage reference with 0.065%/V line sensitivity. International Journal of Circuit Theory and Applications, 2015, 43, 421-426.	1.3	5
121	Transients during pre-breakdown and hard breakdown of thin gate oxides in metalâ€“SiO2â€“Si capacitors. Materials Science in Semiconductor Processing, 1999, 2, 359-367.	1.9	4
122	Two-channel amplifier for high-sensitivity voltage noise measurements. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2007, , .	0.0	4
123	Interfacial layer quality effects on low-frequency noise (1/f) in p-MOSFETs with advanced gate stacks. Microelectronics Reliability, 2007, 47, 501-504.	0.9	4
124	Performance of current mirror with high-k gate dielectrics. Microelectronic Engineering, 2008, 85, 284-288.	1.1	4
125	Electron transport through electrically induced nanoconstrictions in HfSiON gate stacks. Applied Physics Letters, 2008, 92, 253505.	1.5	4
126	Criticisms on and comparison of experimental channel backscattering extraction methods. Microelectronic Engineering, 2011, 88, 76-81.	1.1	4

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127	Influence of GaN- and Si3N4-Passivation Layers on the Performance of AlGaN/GaN Diodes With a Gated Edge Termination. IEEE Transactions on Electron Devices, 2019, 66, 883-889.	1.6	4
128	Impact of Scaling on Physical Unclonable Function Based on Spinâ€"Orbit Torque. IEEE Magnetics Letters, 2020, 11, 1-5.	0.6	4
129	Making IoT Services Accountable: A Solution Based on Blockchain and Physically Unclonable Functions. Lecture Notes in Computer Science, 2019, , 294-305.	1.0	4
130	Assessment of paper-based MoS2 FET for Physically Unclonable Functions. Solid-State Electronics, 2022, 194, 108391.	0.8	4
131	Performance and reliability of ultra-thin oxide nMOSFETs under variable body bias. Microelectronic Engineering, 2007, 84, 1947-1950.	1.1	3
132	Detection and Classification of Single-Electron Jumps in Si Nanocrystal Memories. IEEE Transactions on Instrumentation and Measurement, 2008, 57, 364-368.	2.4	3
133	Analysis of the impact of rear side geometry on performance of back-contact back-junction solar cells. , 2014, , .		3
134	Single Defect Discharge Events in Vertical-Nanowire Tunnel-FETs. IEEE Transactions on Device and Materials Reliability, 2017, 17, 253-258.	1.5	3
135	Understanding the impact of point-contact scheme and selective emitter in a c-Si BC-BJ solar cell by full 3D numerical simulations. Solar Energy, 2017, 155, 1443-1450.	2.9	3
136	Design of a sub-1-V nanopower CMOS current reference. , 2017, , .		3
137	Low energy/delay overhead level shifter for wideâ€range voltage conversion. International Journal of Circuit Theory and Applications, 2017, 45, 1637-1646.	1.3	3
138	Simulations and comparisons of basic analog and digital circuit blocks employing Tunnel FETs and conventional FinFETs. , 2017, , .		3
139	A variation-aware simulation framework for hybrid CMOS/spintronic circuits. , 2017, , .		3
140	Assessment of 2D-FET Based Digital and Analog Circuits on Paper. Solid-State Electronics, 2021, 185, 108063.	0.8	3
141	Extraction of the trap distribution responsible for SILCs in MOS structures from the measurements and simulations of DC and noise properties. Microelectronics Reliability, 2004, 44, 1497-1501.	0.9	2
142	Low frequency noise in nMOSFETs with subnanometer EOT hafnium-based gate dielectrics. Microelectronics Reliability, 2007, 47, 2109-2113.	0.9	2
143	A Comparative Study of MWT Architectures by Means of Numerical Simulations. Energy Procedia, 2013, 38, 131-136.	1.8	2
144	Understanding the Optimization of the Emitter Coverage in BC-BJ Solar Cells. Energy Procedia, 2015, 77, 149-152.	1.8	2

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145	Measurements and Simulations on the Mechanisms of Efficiency Losses in HIT Solar Cells. International Journal of Photoenergy, 2015, 2015, 1-7.	1.4	2
146	Design guidelines for a metallization scheme with multiple-emitter contact lines in BC-BJ solar cells. Journal of Computational Electronics, 2016, 15, 1498-1504.	1.3	2
147	Electrical Characterization of the Influence of the Annealing Energy Density on Carrier Lifetimes in Germanium. ECS Journal of Solid State Science and Technology, 2016, 5, P3013-P3017.	0.9	2
148	Chip/Package/Board Co-Simulation Methodology for Crosstalk between DC/DC Converter and ADC Input Channels. , 2018, , .		2
149	Reliability in GaN-based devices for power applications. , 2018, , .		2
150	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops. , 2019, , .		2
151	Adjusting thermal stability in double-barrier MTJ for energy improvement in cryogenic STT-MRAMs. Solid-State Electronics, 2022, 194, 108315.	0.8	2
152	Smart Material Implication Using Spin-Transfer Torque Magnetic Tunnel Junctions for Logic-in-Memory Computing. Solid-State Electronics, 2022, 194, 108390.	0.8	2
153	A Procedure For Extracting 1/f Noise From Random Telegraph Signals. Conference Record - IEEE Instrumentation and Measurement Technology Conference, 2007, , .	0.0	1
154	Multiple gate NVM cells with improved Fowlerâ€"Nordheim tunneling program and erase performances. Solid-State Electronics, 2010, 54, 1319-1325.	0.8	1
155	Experimental study of leakage-delay trade-off in Germanium pMOSFETs for logic circuits. , 2010, , .		1
156	Experimental analysis of buried SiGe pMOSFETs from the perspective of aggressive voltage scaling. , 2011, , .		1
157	Wafer Level Statistical Evaluation of the Proton Radiation Hardness of a High-k Dielectric/Metal Gate 45 nm Bulk CMOS Technology. ECS Transactions, 2013, 50, 213-222.	0.3	1
158	Early assessment of tunnel-FET for energy-efficient logic circuits. , 2016, , .		1
159	Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory. , 2019, , .		1
160	Modeling pFET currents after soft breakdown at different gate locations. Microelectronic Engineering, 2004, 72, 125-129.	1.1	0
161	Impact of the variable output resistance on the transient response of LC transmission line CMOS buffers and its model. Microwave and Optical Technology Letters, 2007, 49, 1504-1509.	0.9	0
162	Comparison of stressed Poly-Si and TiN gated Hf-based NMOSFETs characteristics, modeling and their impact on circuits performance. Microelectronic Engineering, 2007, 84, 2113-2116.	1.1	0

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163	Forward to the Special Section on â€œReliability of High-Mobility Channel Materialsâ€ IEEE Transactions on Device and Materials Reliability, 2013, 13, 428-428.	1.5	0
164	A virtual III-V tunnel FET technology platform for ultra-low voltage comparators and level shifters. , 2017, , .		0
165	Impact of the Emitter Contact Pattern in c-Si BC- BJ Solar Cells by Numerical Simulations. , 2018, , .		0
166	Design of a 3T current reference for low-voltage, low-power operation. , 2018, , .		0
167	Package Design Methodology for Crosstalk Mitigation between DC/DC Converter and ADC Analog Inputs in Complex SoC. , 2019, , .		0
168	Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers. , 2019, , .		0