Yongpan Liu

List of Publications by Year
in descending order

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121 papers	3,309 citations	361296 20 h-index	254106 43 g-index
121 all docs	121 docs citations	121 times ranked	2286 citing authors

#	Article	IF	Citations
1	PRIME. Computer Architecture News, 2016, 44, 27-39.	2.5	823
2	PRIME: A Novel Processing-in-Memory Architecture for Neural Network Computation in ReRAM-Based Main Memory. , 2016, , .		238
3	Architecture exploration for ambient energy harvesting nonvolatile processors. , 2015, , .		174
4	Accurate Temperature-Dependent Integrated Circuit Leakage Power Estimation is Easy. , 2007, , .		135
5	A 3us wake-up time nonvolatile processor based on ferroelectric flip-flops. , 2012, , .		129
6	Thermal vs Energy Optimization for DVFS-Enabled Processors in Embedded Systems. , 2007, , .		94
7	Storage-Less and Converter-Less Photovoltaic Energy Harvesting With Maximum Power Point Tracking for Internet of Things. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 173-186.	1.9	87
8	Sticker: A 0.41-62.1 TOPS/W 8Bit Neural Network Processor with Multi-Sparsity Compatible Convolution Arrays and Online Tuning Acceleration for Fully Connected Layers. , 2018, , .		86
9	GraphH: A Processing-in-Memory Architecture for Large-Scale Graph Processing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 640-653.	1.9	75
10	Fixing the broken time machine. , 2015, , .		64
11	Nonvolatile Processor Architecture Exploration for Energy-Harvesting Applications. IEEE Micro, 2015, 35, 32-40.	1.8	58
12	STICKER: An Energy-Efficient Multi-Sparsity Compatible Accelerator for Convolutional Neural Networks in 65-nm CMOS. IEEE Journal of Solid-State Circuits, 2020, 55, 465-477.	3.5	51
13	Storage-less and converter-less maximum power point tracking of photovoltaic cells for a nonvolatile microprocessor. , 2014, , .		49
14	Advancing Nonvolatile Computing With Nonvolatile NCFET Latches and Flip-Flops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2907-2919.	3.5	49
15	Design of Nonvolatile SRAM with Ferroelectric FETs for Energy-Efficient Backup and Restore. IEEE Transactions on Electron Devices, 2017, 64, 3037-3040.	1.6	48
16	Utilizing PCM for Energy Optimization in Embedded Systems. , 2012, , .		45
17	Hardware Trojan Detection in Third-Party Digital Intellectual Property Cores by Multilevel Feature Analysis. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1370-1383.	1.9	42
18	PaCC: A Parallel Compare and Compress Codec for Area Reduction in Nonvolatile Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1491-1505.	2.1	41

#	Article	IF	Citations
19	A ReRAM-Based Nonvolatile Flip-Flop With Self-Write-Termination Scheme for Frequent-OFF Fast-Wake-Up Nonvolatile Processors. IEEE Journal of Solid-State Circuits, 2017, 52, 2194-2207.	3.5	41
20	Incidental computing on IoT nonvolatile processors. , 2017, , .		38
21	A compare-and-write ferroelectric nonvolatile flip-flop for energy-harvesting applications. , 2010, , .		35
22	A Ferroelectric Nonvolatile Processor with 46 $mu $ s System-Level Wake-up Time and 14 $mu $ s Sleep Time for Energy Harvesting Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 596-607.	3.5	35
23	Universal Compact Model for Thin-Film Transistors and Circuit Simulation for Low-Cost Flexible Large Area Electronics. IEEE Transactions on Electron Devices, 2017, 64, 2030-2037.	1.6	31
24	Demystifying and Mitigating Code-Dependent Switching Distortions in Current-Steering DACs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 68-81.	3.5	28
25	Solar Power Prediction Assisted Intra-task Scheduling for Nonvolatile Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 724-737.	1.9	26
26	Design of 2T/Cell and 3T/Cell Nonvolatile Memories with Emerging Ferroelectric FETs. IEEE Design and Test, 2019, 36, 39-45.	1.1	26
27	Compiler directed automatic stack trimming for efficient non-volatile processors. , 2015, , .		25
28	Efficient and Robust Nonvolatile Computing-In-Memory Based on Voltage Division in 2T2R RRAM With Input-Dependent Sensing Control. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1640-1644.	2.2	25
29	Stack-Size Sensitive On-Chip Memory Backup for Self-Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1804-1816.	1.9	24
30	A General Framework for Hardware Trojan Detection in Digital Circuits by Statistical Learning Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1633-1646.	1.9	23
31	SPaC: A Segment-based Parallel Compression for Backup Acceleration in Nonvolatile Processors. , 2013, , .		22
32	Lowering Area Overheads for FeFET-Based Energy-Efficient Nonvolatile Flip-Flops. IEEE Transactions on Electron Devices, 2018, 65, 2670-2674.	1.6	21
33	A 3.77TOPS/W Convolutional Neural Network Processor With Priority-Driven Kernel Optimization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 277-281.	2.2	21
34	Data Backup Optimization for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1660-1673.	1.9	20
35	An Energy Efficient Backup Scheme with Low Inrush Current for Nonvolatile SRAM in Energy Harvesting Sensor Nodes. , 2015, , .		19
36	Software Assisted Non-volatile Register Reduction for Energy Harvesting Based Cyber-Physical System. , 2015, , .		19

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37	Spendthrift: Machine learning based resource and frequency scaling for ambient energy harvesting nonvolatile processors. , 2017, , .		18
38	Dynamic Power and Energy Management for Energy Harvesting Nonvolatile Processor Systems. Transactions on Embedded Computing Systems, 2017, 16, 1-23.	2.1	18
39	An Ultracompact Switching-Voltage-Based Fully Reconfigurable RRAM PUF With Low Native Instability. IEEE Transactions on Electron Devices, 2020, 67, 3010-3013.	1.6	18
40	Enabling Lower-Power Charge-Domain Nonvolatile In-Memory Computing With Ferroelectric FETs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2262-2266.	2.2	18
41	STICKER-IM: A 65 nm Computing-in-Memory NN Processor Using Block-Wise Sparsity Optimization and Inter/Intra-Macro Data Reuse. IEEE Journal of Solid-State Circuits, 2022, 57, 2560-2573.	3.5	17
42	Dynamic machine learning based matching of nonvolatile processor microarchitecture to harvested energy profile. , 2015, , .		16
43	Wear-Leveling Aware Page Management for Non-Volatile Main Memory on Embedded Systems. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 129-142.	2.5	16
44	A Bidirectional Integrated Equalizer Based on the Sepicâ€“Zeta Converter for Hybrid Energy Storage System. IEEE Transactions on Power Electronics, 2022, 37, 12659-12668.	5.4	16
45	A ReRAM-Based Computing-in-Memory Convolutional-Macro With Customized 2T2R Bit-Cell for AIoT Chip IP Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 1534-1538.	2.2	15
46	FeFET-based low-power bitwise logic-in-memory with direct write-back and data-adaptive dynamic sensing interface. , 2020, , .		14
47	Intra-task scheduling for storage-less and converter-less solar-powered nonvolatile sensor nodes. , 2014, , .		13
48	Design exploration of inrush current aware controller for nonvolatile processor. , 2015, , .		13
49	A 130-nm Ferroelectric Nonvolatile System-on-Chip With Direct Peripheral Restore Architecture for Transient Computing System. IEEE Journal of Solid-State Circuits, 2019, 54, 885-895.	3.5	13
50	Design methodology of variable latency adders with multistage function speculation. , 2010, , .		12
51	Maximum Energy Efficiency Tracking Circuits for Converter-Less Energy Harvesting Sensor Nodes. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 670-674.	2.2	12
52	A Novel General Compact Model Approach for 7-nm Technology Node Circuit Optimization From Device Perspective and Beyond. IEEE Journal of the Electron Devices Society, 2020, 8, 295-301.	1.2	12
53	StructADMM: Achieving Ultrahigh Efficiency in Structured Pruning for DNNs. IEEE Transactions on Neural Networks and Learning Systems, 2022, 33, 2259-2273.	7.2	12
54	PATH: Performance-Aware Task Scheduling for Energy-Harvesting Nonvolatile Processors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1671-1684.	2.1	11

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55	Dynamic Channel Modeling and OFDM System Analysis for Capacitive Coupling Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 735-745.	2.7	11
56	A Sparse-Adaptive CNN Processor with Area/Performance balanced N-Way Set-Associate PE Arrays Assisted by a Collision-Aware Scheduler. , 2019, , .		11
57	Checkpointing-Aware Loop Tiling for Energy Harvesting Powered Nonvolatile Processors. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 15-28.	1.9	11
58	CORAL: Coarse-grained reconfigurable architecture for Convolutional Neural Networks. , 2017, , .		10
59	An Auto Loss Compensation System for Capacitive-Coupled Body Channel Communication. IEEE Transactions on Biomedical Circuits and Systems, 2019, 13, 756-765.	2.7	10
60	High PE Utilization CNN Accelerator with Channel Fusion Supporting Pattern-Compressed Sparse Neural Networks. , 2020, , .		10
61	A precision adaptive average time synchronization protocol in wireless sensor networks. , 2008, , .		9
62	Noise Margin Modeling for Zero-$V_{ext {GS}}$ Load TFT Circuits and Yield Estimation. IEEE Transactions on Electron Devices, 2016, 63, 684-690.	1.6	9
63	A 4-Mbps 41-pJ/bit On-off Keying Transceiver for Body-channel Communication with Enhanced Auto Loss Compensation Technique. , 2019, , .		9
64	Lightweight Precision-Adaptive Time Synchronization in Wireless Sensor Networks. IEICE Transactions on Communications, 2010, E93-B, 2299-2308.	0.4	8
65	Multi-source energy harvesting management and optimization for non-volatile processors. , 2015, , .		8
66	Multi-source in-door energy harvesting for non-volatile processors. , 2016, , .		8
67	A 65-nm ReRAM-Enabled Nonvolatile Processor With Time-Space Domain Adaption and Self-Write-Termination Achieving $> 4imes $ Faster Clock Frequency and $> 6imes $ Higher Restore Speed. IEEE Journal of Solid-State Circuits, 2017, 52, 2769-2785.	3.5	8
68	A 3T/Cell Practical Embedded Nonvolatile Memory Supporting Symmetric Read and Write Access Based on Ferroelectric FETs. , 2019, , .		7
69	MaxTracker: Continuously Tracking the Maximum Computation Progress for Energy Harvesting ReRAM-based CNN Accelerators. Transactions on Embedded Computing Systems, 2021, 20, 1-23.	2.1	7
70	NVPsim: A simulator for architecture explorations of nonvolatile processors. , 2016, , .		6
71	DVFS-Based Long-Term Task Scheduling for Dual-Channel Solar-Powered Sensor Nodes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2981-2994.	2.1	6
72	A 2.2-GHz Configurable Direct Digital Frequency Synthesizer Based on LUT and Rotation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1970-1980.	3.5	6

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73	STICKER-T: An Energy-Efficient Neural Network Processor Using Block-Circulant Algorithm and Unified Frequency-Domain Acceleration. IEEE Journal of Solid-State Circuits, 2021, 56, 1936-1948.	3.5	6
74	High-Quality Single-Model Deep Video Compression with Frame-Conv3D and Multi-frame Differential Modulation. Lecture Notes in Computer Science, 2020, , 239-254.	1.0	6
75	Design Insights of Non-volatile Processors and Accelerators in Energy Harvesting Systems. , 2020, , .		6
76	An energy efficient fully integrated OOK transceiver SoC for wireless body area networks. , 2013, , .		5
77	Noise Margin, Delay, and Power Model for Pseudo-CMOS TFT Logic Circuits. IEEE Transactions on Electron Devices, 2017, 64, 2635-2642.	1.6	5
78	CP-FPGA: Energy-Efficient Nonvolatile FPGA With Offline/Online Checkpointing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2153-2163.	2.1	5
79	'The danger of sleeping', an exploration of security in non-volatile processors. , 2017, , .		5
80	Efficient energy management by exploiting retention state for self-powered nonvolatile processors. Journal of Systems Architecture, 2018, 87, 23-35.	2.5	5
81	AERIS. , 2019, , .		5
82	Lifetime-Aware Battery Allocation for Wireless Sensor Network under Cost Constraints. IEICE Transactions on Communications, 2012, E95.B, 1651-1660.	0.4	5
83	Performance-centric register file design for GPUs using racetrack memory. , 2016, , .		4
84	Accuracy Optimization With the Framework of Non-Volatile Computing-In-Memory Systems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 518-529.	3.5	4
85	PACA: A Pattern Pruning Algorithm and Channel-Fused High PE Utilization Accelerator for CNNs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 5043-5056.	1.9	4
86	Nonvolatile memory allocation and hierarchy optimization for high-level synthesis. , 2015, , .		3
87	A Dual-Threshold Scheme Along with Security Reinforcement for Energy Efficient Nonvolatile Processors. , 2018, , .		3
88	Reliability and Security in Non-volatile Processors, Two Sides of the Same Coin. , 2018, , .		3
89	Low Overhead Online Checkpoint for Intermittently Powered Non-volatile FPGAs. , 2018, , .		3
90	Accelerating CNN-RNN Based Machine Health Monitoring on FPGA. , 2019, , .		3

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91	Investigation and Modeling of Multi-Node Body Channel Wireless Power Transfer. Sensors, 2020, 20, 156.	2.1	3
92	One-Shot Refresh: A Low-Power Low-Congestion Approach for Dynamic Memories. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3402-3406.	2.2	3
93	Leakage Power Modeling Method for SRAM Considering Temperature, Supply Voltage and Bias Voltage. , 2006, , .		2
94	Improved adaptive compression arbitration system for wireless sensor networks. Tsinghua Science and Technology, 2010, 15, 202-208.	4.1	2
95	Accurate personal ultraviolet dose estimation with multiple wearable sensors. , 2016, , .		2
96	Design Methodology for Thin-Film Transistor Based Pseudo-CMOS Logic Array with Multi-Layer Interconnect Architecture. , 2017, , .		2
97	Prototyping Energy Harvesting Powered Systems with Nonvolatile Processor (Invited Paper). , 2018, , .		2
98	GAAS: An Efficient Group Associated Architecture and Scheduler Module for Sparse CNN Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5170-5182.	1.9	2
99	Block-Circulant Neural Network Accelerator Featuring Fine-Grained Frequency-Domain Quantization and Reconfigurable FFT Modules. , 2021, , .		2
100	DyTAN: Dynamic Ternary Content Addressable Memory Using Nanoelectromechanical Relays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1981-1993.	2.1	2
101	Multi-channel precision-sparsity-adapted inter-frame differential data codec for video neural network processor. , 2020, , .		2
102	A 65-nm Energy-Efficient Interframe Data Reuse Neural Network Accelerator for Video Applications. IEEE Journal of Solid-State Circuits, 2022, 57, 2574-2585.	3.5	2
103	Dynamic CNN Accelerator Supporting Efficient Filter Generator with Kernel Enhancement and Online Channel Pruning. , 2022, , .		2
104	Bit-Aware Fault-Tolerant Hybrid Retraining and Remapping Schemes for RRAM-Based Computing-in-Memory Systems. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3144-3148.	2.2	2
105	Design methodology of multistage time-domain logic speculation circuits. , 2011, , .		1
106	A low-complexity symbol-level differential detection scheme for IEEE 802.15.4 O-QPSK signals. , 2012, , .		1
107	Optimal partition with block-level parallelization in C-to-RTL synthesis for streaming applications. , 2013, , .		1
108	A novel hybrid storage architecture for nonvolatile FPGA. , 2014, , .		1

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109	Using nonvolatile processors to reduce leakage in power management approaches. , 2014, , .		1
110	Simultaneous accelerator parallelization and point-to-point interconnect insertion for bus-based embedded SoCs. Tsinghua Science and Technology, 2015, 20, 644-660.	4.1	1
111	Dynamic converter reconfiguration for near-threshold non-volatile processors using in-door energy harvesting. , 2016, , .		1
112	CP-FPGA: Computation data-aware software/hardware co-design for nonvolatile FPGAs based on checkpointing techniques. , 2016, , .		1
113	CNN-based pattern recognition on nonvolatile IoT platform for smart ultraviolet monitoring: (Invited) Tj ETQq1 1 0.784314 rgBT /Ove		1
114	Mechanical strain and temperature aware design methodology for thin-film transistor based pseudo-CMOS logic array. , 2018, , .		1
115	An Investigation on Inter-degeneration Effect in Body Channel Based Multi-node Wireless Power Transfer. , 2018, , .		1
116	Design Methodology for TFT-Based Pseudo-CMOS Logic Array With Multilayer Interconnection Architecture and Optimization Algorithms. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2043-2057.	1.9	1
117	A Non-Volatile Computing-In-Memory Framework With Margin Enhancement Based CSA and Offset Reduction Based ADC. , 2021, , .		1
118	Multistage Function Speculation Adders. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2015, E98.A, 954-965.	0.2	1
119	A New Thermal-Conscious System-Level Methodology for Energy-Efficient Processor Voltage Selection. , 2006, , .		0
120	An Energy Efficient Sensor Network Processor with Latency-Aware Adaptive Compression. IEICE Transactions on Electronics, 2011, E94-C, 1220-1228.	0.3	0
121	Toward Low-Bit Neural Network Training Accelerator by Dynamic Group Accumulation. , 2022, , .		0