

# Hossein Shamsi

## List of Publications by Year in descending order

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papers

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citations

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docs citations

41  
times ranked

233  
citing authors

#	ARTICLE	IF	CITATIONS
1	Design of Unequal Dual Band Gysel Power Divider With Isolation Bandwidth Improvement. IEEE Microwave and Wireless Components Letters, 2017, 27, 138-140.	3.2	34
2	Analog programmable neuron and case study on VLSI implementation of Multi-Layer Perceptron (MLP). Microelectronics Journal, 2019, 84, 36-47.	2.0	24
3	Exploiting cross-coupled and body-driven techniques for noise cancellation of an inductor-less wideband LNA. AEU - International Journal of Electronics and Communications, 2015, 69, 708-714.	2.9	23
4	98-dB Gain Class-AB OTA With 100 pF Load Capacitor in 180-nm Digital CMOS Process. IEEE Access, 2019, 7, 17772-17779.	4.2	19
5	Low Power High Speed Dynamic Comparator. , 2018, , .		16
6	84-dB DC-gain two-stage class-AB OTA. IET Circuits, Devices and Systems, 2019, 13, 614-621.	1.4	13
7	A new two-stage Op-Amp using hybrid cascode compensation, bulk-driven, and positive feedback techniques. , 2010, , .		12
8	On the design of a low-voltage two-stage OTA using bulk-driven and positive feedback techniques. International Journal of Electronics, 2012, 99, 1309-1315.	1.4	11
9	Yield-aware sizing of pipeline ADC using a multiple-objective evolutionary algorithm. International Journal of Circuit Theory and Applications, 2017, 45, 744-763.	2.0	10
10	Resilient design of current steering DACs using a transistor level approach. Analog Integrated Circuits and Signal Processing, 2017, 90, 29-41.	1.4	10
11	Positive feedback technique and split-length transistors for DC-gain enhancement of two-stage op-amps. IET Circuits, Devices and Systems, 2017, 11, 605-612.	1.4	10
12	Design and Implementation of an RFID-GSM-Based Vehicle Identification System on Highways. IEEE Sensors Journal, 2018, 18, 7281-7293.	4.7	10
13	Positive feedback technique for DC-gain enhancement of folded cascode Op-Amps. , 2012, , .		8
14	Digital Calibration of DAC Unit Elements Mismatch in Pipelined ADCs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 34-45.	5.4	8
15	Automatic Design and Yield Enhancement of Data Converters. Journal of Circuits, Systems and Computers, 2017, 26, 1750018.	1.5	7
16	Two-stage class-AB OTA with enhanced DC gain and slew rate. International Journal of Electronics Letters, 2017, 5, 438-448.	1.2	6
17	Three-Dimensional Pipeline ADC Utilizing TSV/ Design Optimization and Memristor Ratioed Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2619-2627.	3.1	6
18	Digital Noise Coupled MASH Delta-Sigma Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 41-45.	3.0	6

#	ARTICLE	IF	CITATIONS
19	A new two-stage Op-Amp using gate-driven, and positive feedback techniques. , 2010, , .		5
20	A Low-Collision CSMA-Based Active RFID for Tracking Applications. Wireless Personal Communications, 2013, 71, 2827-2847.	2.7	5
21	A 10-bit 50-MS/s charge injection pipelined ADC using a digital calibration. , 2012, , .		4
22	Single-layer wideband differential phase shifter using high-order multimode resonator structure. AEU - International Journal of Electronics and Communications, 2020, 115, 153023.	2.9	4
23	Multi-objective design automation of the folded-cascode OP-AMP using NSGA-II Strategy. , 2009, , .		3
24	On the Design of a User Interface for an RFID-Based Vehicle Tracking System. International Journal of Wireless Information Networks, 2017, 24, 56-61.	2.7	3
25	Simple ladder-like single-layer balanced wideband phase shifter with wide phase shift range and appropriate common-mode suppression. IET Microwaves, Antennas and Propagation, 2020, 14, 1137-1147.	1.4	3
26	A 2.4GHz sub 1-mW highly linear differential LNA using balun transformer gm-boosting technique. Microelectronics Journal, 2022, 119, 105280.	2.0	3
27	Extracting trade-off boundaries of CMOS two-stage op-amp using particle swarm optimization. , 2009, , .		2
28	A 109dB PSRR, 31&#x00B5;W fully-MOSFET bandgap voltage reference in 0.13&#x00B5;m CMOS technology. , 2010, , .		2
29	Combination of DAC switches and SAR logics in a 720&#x00A5;MS/s low-bit successive approximation ADC. Analog Integrated Circuits and Signal Processing, 2014, 80, 263-272.	1.4	2
30	Linear doherty power amplifier with enhanced back-off efficiency mode for LTE applications. , 2016, , .		2
31	Modified dual band gysel power divider with isolation bandwidth improvement. , 2016, , .		2
32	Placement and routing method for analogue layout generation using modified cuckoo optimisation algorithm. IET Circuits, Devices and Systems, 2018, 12, 532-541.	1.4	2
33	Low-voltage and low-power Ku-band CMOS LNA using capacitive feedback. Analog Integrated Circuits and Signal Processing, 2021, 109, 435-447.	1.4	2
34	On the design of a less jitter sensitive NTF for NRZ multi-bit continuous-time &#x0394;&#x03A3; modulators. , 2009, , .		1
35	Design of a CMOS LNA for the upper band of UWB receivers. , 2011, , .		1
36	New low-loss tunable microstrip band-pass filter with two transmission zeros. Analog Integrated Circuits and Signal Processing, 2019, 98, 401-408.	1.4	1

#	ARTICLE	IF	CITATIONS
37	On the Design of Highly Efficient Harmonic Tuned Wideband Class F-1/F Power Amplifier. , 2021, , .		1
38	A 400 ps Input Time Range 2 <sup>Å</sup> — Time Amplifier Using Time-to-Current Compensation Technique. , 2021, , .		1
39	A 5-GHZ VCO for WLAN applications. , 2010, , .		0
40	Performance enhancement of a 10-Bit 50-MS/s open loop pipelined ADC using a novel digital calibration. , 2012, , .		0
41	A bipolar offset binary time-to-digital converter using time amplifiers based on time-to-current compensation. AEU - International Journal of Electronics and Communications, 2022, 144, 154072.	2.9	0