Gregory K Chen

List of Publications by Year
in descending order

7 papers	271 citations	1937685 4 h-index	1872680 6 g-index
7 all docs	7 docs citations	7 times ranked	287 citing authors

#	Article	IF	Citations
1	A 617-TOPS/W All-Digital Binary Neural Network Accelerator in 10-nm FinFET CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 1082-1092.	5.4	17
2	A 4900-mu m² 839-Mb/s Side-Channel Attack- Resistant AES-128 in 14-nm CMOS With Heterogeneous Sboxes, Linear Masked MixColumns, and Dual-Rail Key Addition. IEEE Journal of Solid-State Circuits, 2020, 55, 945-955.	5.4	13
3	A 2.9â€“33.0 TOPS/W Reconfigurable 1-D/2-D Compute-Near-Memory Inference Accelerator in 10-nm FinFET CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 118-121.	2.0	4
4	A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS. , 2020, , .		17
5	A 9.0-TOPS/W Hash-Based Deep Neural Network Accelerator Enabling 128Ã— Model Compression in 10-nm FinFET CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 338-341.	2.0	2
6	A 4096-Neuron 1M-Synapse 3.8-pJ/SOP Spiking Neural Network With On-Chip STDP Learning and Sparse Weights in 10-nm FinFET CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 992-1002.	5.4	119
7	340 mVâ€“1.1 V, 289 Gbps/W, 2090-Gate NanoAES Hardware Accelerator With Area-Optimized Encrypt/Decrypt GF(2 4) 2 Polynomials in 22 nm Tri-Gate CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 1048-1058.	5.4	99