

Gregory K Chen

List of Publications by Year in descending order

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| # | ARTICLE | IF | CITATIONS |
|---|--|-----|-----------|
| 1 | A 4096-Neuron 1M-Synapse 3.8-pJ/SOP Spiking Neural Network With On-Chip STDP Learning and Sparse Weights in 10-nm FinFET CMOS. IEEE Journal of Solid-State Circuits, 2019, 54, 992-1002. | 5.4 | 119 |
| 2 | 340 mV@1.1 V, 289 Gbps/W, 2090-Gate NanoAES Hardware Accelerator With Area-Optimized Encrypt/Decrypt GF(2 ⁴) ² Polynomials in 22 nm Tri-Gate CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 1048-1058. | 5.4 | 99 |
| 3 | A 617 TOPS/W All Digital Binary Neural Network Accelerator in 10nm FinFET CMOS. , 2020, , . | | 17 |
| 4 | A 617-TOPS/W All-Digital Binary Neural Network Accelerator in 10-nm FinFET CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 1082-1092. | 5.4 | 17 |
| 5 | A 4900- μm^2 839-Mb/s Side-Channel Attack-Resistant AES-128 in 14-nm CMOS With Heterogeneous Sboxes, Linear Masked MixColumns, and Dual-Rail Key Addition. IEEE Journal of Solid-State Circuits, 2020, 55, 945-955. | 5.4 | 13 |
| 6 | A 2.9@33.0 TOPS/W Reconfigurable 1-D/2-D Compute-Near-Memory Inference Accelerator in 10-nm FinFET CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 118-121. | 2.0 | 4 |
| 7 | A 9.0-TOPS/W Hash-Based Deep Neural Network Accelerator Enabling 128-Model Compression in 10-nm FinFET CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 338-341. | 2.0 | 2 |