

Ahmad Hiasat

List of Publications by Year in descending order

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27
times ranked

113
citing authors

#	ARTICLE	IF	CITATIONS
1	High-speed and reduced-area modular adder structures for RNS. IEEE Transactions on Computers, 2002, 51, 84-89.	3.4	78
2	VLSI implementation of new arithmetic residue to binary decoders. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 153-158.	3.1	46
3	New efficient structure for a modular multiplier for RNS. IEEE Transactions on Computers, 2000, 49, 170-174.	3.4	44
4	Residue number system to binary converter for the moduli set $(2n^{\wedge}1, 2n^{\wedge}1, 2n+1)$. Journal of Systems Architecture, 2003, 49, 53-58.	4.3	21
5	A Suggestion for a Fast Residue Multiplier for a Family of Moduli of the Form $(2n - (2p \wedge 1))$. Computer Journal, 2004, 47, 93-102.	2.4	19
6	Efficient RNS Scalers for the Extended Three-Moduli Set $(2^{\wedge}\{n\}-1, 2^{\wedge}\{n+p\}, 2^{\wedge}\{n+1\})$. IEEE Transactions on Computers, 2017, 66, 1253-1260.	3.4	19
7	Combinational logic approach for implementing an improved approximate squaring function. IEEE Journal of Solid-State Circuits, 1999, 34, 236-240.	5.4	18
8	A Reverse Converter and Sign Detectors for an Extended RNS Five-Moduli Set. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 111-121.	5.4	18
9	A Residue-to-Binary Converter for the Extended Four-Moduli Set $(2^{\wedge}\{n\}-1, 2^{\wedge}\{n+1\}, 2^{\wedge}\{2n\}+1, 2^{\wedge}\{2n+p\})$. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2188-2192.	3.1	16
10	A Sign Detector for a Group of Three-Moduli Sets. IEEE Transactions on Computers, 2016, 65, 3580-3590.	3.4	14
11	Bit-serial architecture for rank order and stack filters. The Integration VLSI Journal, 2003, 36, 3-12.	2.1	13
12	An Efficient Reverse Converter for the Three-Moduli Set $(2^{\wedge}\{n+1\}-1, 2^{\wedge}\{n\}, 2^{\wedge}\{n\}-1)$. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 962-966.	3.0	12
13	Sign detector for the extended four-moduli set. IET Computers and Digital Techniques, 2018, 12, 39-43.	1.2	11
14	General modular adder designs for residue number system applications. IET Circuits, Devices and Systems, 2018, 12, 424-431.	1.4	11
15	On the Design of RNS Inter-Modulo Processing Units for the Arithmetic-Friendly Moduli Sets $\{2^{\wedge}\{n\}+1, 2^{\wedge}\{n\}-1, 2^{\wedge}\{n\}+1\}$. Computer Journal, 2019, 62, 292-300.	2.4	11
16	Semi-Custom VLSI Design and Implementation of a New Efficient RNS Division Algorithm. Computer Journal, 1999, 42, 232-240.	2.4	10
17	A Residue-to-Binary Converter with an Adjustable Structure for an Extended RNS Three-Moduli Set. Journal of Circuits, Systems and Computers, 2019, 28, 1950126.	1.5	10
18	New Residue Number System Scaler for the Three-Moduli Set $\{2n+1, 2n, 2n-1\}$. Computers, 2018, 7, 46.	3.3	9

#	ARTICLE	IF	CITATIONS
19	Sign Identifier for the Enhanced Three Moduli Set $\{2n + k, 2n\hat{a}^{\%1}, 2n+\hat{a}^{\%1}\hat{a}^{\%1}\}$. Journal of Signal Processing Systems, 2019, 91, 953-961.	2.1	7
20	A Scaler Design for the RNS Three-Moduli Set $\{2n+1\hat{a}^1, 2n, 2n\hat{a}^1\}$ Based on Mixed-Radix Conversion. Journal of Circuits, Systems and Computers, 2020, 29, 2050041.	1.5	7
21	A Reverse Converter for Three-Moduli Set $(2k, 2n - 1, 2n + 1)$, $k < n$. , 2019, , .		4
22	General Frameworks for Designing Arithmetic Components for Residue Number Systems. Advances in Intelligent Systems and Computing, 2021, , 82-92.	0.6	1
23	A New Scaler for the Expanded 4-Moduli Set $\{2^{k/sup} \hat{a}^1, 2^{k/sup} + 1, 2^{2k/sup} + 1, 2^{2k/sup}\}$. , 2020, , . An arithmetic scaler circuit design for the expanded four-moduli set <mml:math xmlns:mml="http://www.w3.org/1998/Math/MathML" display="inline" id="d1e1216" altimg="si391.svg"><mml:mrow><mml:mo>{</mml:mo><mml:msup><mml:mrow><mml:mrow><mml:mn>2</mml:mn></mml:mrow></mml:msup><mml:mrow><mml:mrow><mml:mn>2</mml:mn></mml:mrow></mml:mrow></mml:math> linebreak="goodbreak" linebreakstyle="after"></mml:mo><mml:mn>1</mml:mn></mml:mo></mml:mo><mml:msup><mml:mrow><mml:mn>2</mml:mn></mml:mrow></mml:msup>		1
24	Line. Computers and Electrical Engineering, 2022, 101, 108102.	4.8	1
25	limiter discriminator detection of narrow-band duobinary FSK in a land mobile channel. International Journal of Communication Systems, 2004, 17, 85-97.	2.5	0
26	A Modulo $2^{n-2^{n-2}}-1$ Adder Design. Lecture Notes in Networks and Systems, 2021, , 789-802.	0.7	0