Ignacio Algredo-Badillo

List of Publications by Year
in descending order

32	211	1163117 8	1125743 13
papers	citations	h-index	g-index

33	33	33	159
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Trade-Off Analysis of Hardware Architectures for Channel-Quality Classification Models. Sensors, 2022, 22, 2497.	3.8	0
2	Machine Learning Methods Modeling Carbohydrate-Enriched Cyanobacteria Biomass Production in Wastewater Treatment Systems. Energies, 2022, 15, 2500.	3.1	22
3	A Cloud Microservices Architecture for Data Integrity Verifiability Based on Blockchain. Applied Sciences (Switzerland), 2022, 12, 2754.	2.5	3
4	Analysis of Statistical and Artificial Intelligence Algorithms for Real-Time Speed Estimation Based on Vehicle Detection with YOLO. Applied Sciences (Switzerland), 2022, 12, 2907.	2.5	13
5	An SHA-3 Hardware Architecture against Failures Based on Hamming Codes and Triple Modular Redundancy. Sensors, 2022, 22, 2985.	3.8	3
6	A SHA-256 Hybrid-Redundancy Hardware Architecture for Detecting and Correcting Errors. Sensors, 2022, 22, 5028.	3.8	2
7	Bit-Vector-Based Hardware Accelerator for DNA Alignment Tools. Journal of Circuits, Systems and Computers, 2021, 30, 2150087.	1.5	4
8	Bayesian Approach to Analyze Reading Comprehension: A Case Study in Elementary School Children in Mexico. Sustainability, 2021, 13, 4285.	3.2	0
9	Reactive Obstacleâ€“Avoidance Systems for Wheeled Mobile Robots Based on Artificial Intelligence. Applied Sciences (Switzerland), 2021, 11, 6468.	2.5	4
10	A Channel-Quality Classification Analysis for IoT Communication based on Machine Learning. , 2021, , .		0
11	Hybrid Pipeline Hardware Architecture Based on Error Detection and Correction for AES. Sensors, 2021, 21, 5655.	3.8	4
12	CMOS Implementation of ANNs Based on Analog Optimization of N-Dimensional Objective Functions. Sensors, 2021, 21, 7071.	3.8	3
13	RootLogChain: Registering Log-Events in a Blockchain for Audit Issues from the Creation of the Root. Sensors, 2021, 21, 7669.	3.8	2
14	A fuzzy petri net model for assessing analogical reasoning in children ranging from 5 to 8 years old. Journal of Intelligent and Fuzzy Systems, 2020, 39, 7161-7175.	1.4	0
15	An FPGA-based analysis of trade-offs in the presence of ill-conditioning and different precision levels in computations. PLoS ONE, 2020, 15, e0234293.	2.5	2
16	A Metaheuristic Optimization Approach for Parameter Estimation in Arrhythmia Classification from Unbalanced Data. Sensors, 2020, 20, 3139.	3.8	10
17	Real time FPGA-ANN architecture for outdoor obstacle detection focused in road safety. Journal of Intelligent and Fuzzy Systems, 2019, 36, 4425-4436.	1.4	4
18	Reconfigurable arithmetic logic unit designed with threshold logic gates. IET Circuits, Devices and Systems, 2019, 13, 21-30.	1.4	4

#	Article	IF	Citations
19	Lightweight Security Hardware Architecture Using DWT and AES Algorithms. IEICE Transactions on Information and Systems, 2018, E101.D, 2754-2761.	0.7	4
20	On-road obstacle detection video system for traffic accident prevention. Journal of Intelligent and Fuzzy Systems, 2018, 35, 533-547.	1.4	8
21	Compact FPGA hardware architecture for public key encryption in embedded devices. PLoS ONE, 2018, 13, e0190939.	2.5	15
22	A compact FPGA-based processor for the Secure Hash Algorithm SHA-256. Computers and Electrical Engineering, 2014, 40, 194-202.	4.8	35
23	A programmable FPGA-based cryptoprocessor for bilinear pairings over F<inf>2m</inf>. , 2013, , .		0
24	Throughput and Efficiency Analysis of Unrolled Hardware Architectures for the SHA-512 Hash Algorithm. , 2012, , .		5
25	Novel Hardware Architecture for Implementing the Inner Loop of the SHA-2 Algorithms. , 2011, , .		3
26	Efficient hardware architecture for the AES-CCM protocol of the IEEE 802.11i standard. Computers and Electrical Engineering, 2010, 36, 565-577.	4.8	22
27	An area/performance trade-off analysis of a GF(2m) multiplier architecture for elliptic curve cryptography. Computers and Electrical Engineering, 2009, 35, 54-58.	4.8	9
28	A Run Time Reconfigurable Co-processor for Elliptic Curve Scalar Multiplication. , 2009, , .		0
29	FPGA implementation cost and performance evaluation of the IEEE 802.16e and IEEE 802.11i security architectures based on AES-CCM. , 2008, , .		7
30	FPGA Implementation and Performance Evaluation of AES-CCM Cores for Wireless Networks. , 2008, , .		12
31	Design and Implementation of an FPGA-Based 1.452-Gbps Non-pipelined AES Architecture. Lecture Notes in Computer Science, 2006, , 456-465.	1.3	11
32	Analysis of stress and anxiety in university students to identify correlated factors. Revista Teorìa EducativaÂ, 0, , 10-19.	0.0	0