Haruo Shimamoto

List of Publications by Year
in descending order

5	49	2258059 3	2550090 3
papers	citations	h-index	g-index

5	5	5	11
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. IEEE Transactions on Electron Devices, 2021, 68, 2077-2082.	3.0	14
2	Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2747-2755.	5.4	17
3	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 502-510.	2.5	11
4	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. , 2019, , .		5
5	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs. , 2019, , .		2