

Haruo Shimamoto

List of Publications by Year in descending order

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papers

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2258059

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2550090

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docs citations

5
times ranked

11
citing authors

#	ARTICLE	IF	CITATIONS
1	Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. IEEE Journal of Solid-State Circuits, 2020, 55, 2747-2755.	5.4	17
2	3-D CMOS Chip Stacking for Security ICs Featuring Backside Buried Metal Power Delivery Networks With Distributed Capacitance. IEEE Transactions on Electron Devices, 2021, 68, 2077-2082.	3.0	14
3	A Thick Cu Layer Buried in Si Interposer Backside for Global Power Routing. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 502-510.	2.5	11
4	A Si-Backside Protection Circuits Against Physical Security Attacks on Flip-Chip Devices. , 2019, , .		5
5	Over-the-top Si Interposer Embedding Backside Buried Metal PDN to Reduce Power Supply Impedance of Large Scale Digital ICs. , 2019, , .		2