Jae-Sun Seo

List of Publications by Year
in descending order

77 papers	2,447 citations	361413 20 h-index	395702 33 g-index
78 all docs	78 docs citations	78 times ranked	1912 citing authors

#	Article	IF	Citations
1	Optimizing Loop Operation and Dataflow in FPGA Acceleration of Deep Convolutional Neural Networks. , 2017, , .		244
2	Optimizing the Convolution Operation to Accelerate Deep Neural Networks on FPGA. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1354-1367.	3.1	225
3	XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks. IEEE Journal of Solid-State Circuits, 2020, , 1-11.	5.4	189
4	Large-Scale Neuromorphic Spiking Array Processors: A Quest to Mimic the Brain. Frontiers in Neuroscience, 2018, 12, 891.	2.8	177
5	C3SRAM: An In-Memory-Computing SRAM Macro Based on Robust Capacitive Coupling Computing Mechanism. IEEE Journal of Solid-State Circuits, 2020, 55, 1888-1897.	5.4	144
6	XNOR-RRAM: A scalable and parallel resistive synaptic architecture for binary neural networks. , 2018, , .		133
7	XNOR-SRAM: In-Memory Computing SRAM Macro for Binary/Ternary Deep Neural Networks. , 2018, , .		92
8	High-Throughput In-Memory Computing for Binary Deep Neural Networks With Monolithically Integrated RRAM and 90-nm CMOS. IEEE Transactions on Electron Devices, 2020, 67, 4185-4192.	3.0	92
9	An automatic RTL compiler for high-throughput FPGA implementation of diverse deep convolutional neural networks. , 2017, , .		86
10	ALAMO: FPGA acceleration of deep learning algorithms with a modularized RTL compiler. The Integration VLSI Journal, 2018, 62, 14-23.	2.1	68
11	Monolithically Integrated RRAM- and CMOS-Based In-Memory Computing Optimizations for Efficient Deep Learning. IEEE Micro, 2019, 39, 54-63.	1.8	65
12	A 1.06-mu W Smart ECG Processor in 65-nm CMOS for Real-Time Biometric Authentication and Personal Cardiac Monitoring. IEEE Journal of Solid-State Circuits, 2019, 54, 2316-2326.	5.4	53
13	Automatic Compilation of Diverse CNNs Onto High-Performance FPGA Accelerators. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 424-437.	2.7	45
14	Algorithm and hardware design of discrete-time spiking neural networks based on back propagation with binary activations. , 2017, , .		39
15	End-to-end scalable FPGA accelerator for deep residual networks. , 2017, , .		39
16	2-Bit-Per-Cell RRAM-Based In-Memory Computing for Area-/Energy-Efficient Deep Learning. IEEE Solid-State Circuits Letters, 2020, 3, 194-197.	2.0	39
17	C3SRAM: In-Memory-Computing SRAM Macro Based on Capacitive-Coupling Computing. IEEE Solid-State Circuits Letters, 2019, 2, 131-134.	2.0	36
18	An 8.93 TOPS/W LSTM Recurrent Neural Network Accelerator Featuring Hierarchical Coarse-Grain Sparsity for On-Device Speech Recognition. IEEE Journal of Solid-State Circuits, 2020, 55, 1877-1887.	5.4	36

#	ARTICLE	IF	CITATIONS
19	Scalable and modularized RTL compilation of Convolutional Neural Networks onto FPGA. , 2016, , .		34
20	Performance Modeling for CNN Inference Accelerators on FPGA. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 843-856.	2.7	33
21	Vesti: Energy-Efficient In-Memory Computing Accelerator for Deep Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 48-61.	3.1	32
22	Automatic Compiler Based FPGA Accelerator for CNN Training. , 2019, , .		31
23	A Low Ripple Switched-Capacitor Voltage Regulator Using Flying Capacitance Dithering. IEEE Journal of Solid-State Circuits, 2016, 51, 919-929.	5.4	26
24	Structured Pruning of RRAM Crossbars for Efficient In-Memory Computing Acceleration of Deep Neural Networks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1576-1580.	3.0	26
25	Triple-Mode, Hybrid-Storage, Energy Harvesting Power Management Unit: Achieving High Efficiency Against Harvesting and Load Power Variabilities. IEEE Journal of Solid-State Circuits, 2017, 52, 2550-2562.	5.4	25
26	A Latency-Optimized Reconfigurable NoC for In-Memory Acceleration of DNNs. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2020, 10, 362-375.	3.6	25
27	Interconnect-Aware Area and Energy Optimization for In-Memory Acceleration of DNNs. IEEE Design and Test, 2020, 37, 79-87.	1.2	25
28	On-Chip Sparse Learning Acceleration With CMOS and Resistive Synaptic Devices. IEEE Nanotechnology Magazine, 2015, 14, 969-979.	2.0	21
29	Efficient memory compression in deep neural networks using coarse-grain sparsification for speech applications. , 2016, , .		20
30	A 2.6 TOPS/W 16-Bit Fixed-Point Convolutional Neural Network Learning Processor in 65-nm CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 13-16.	2.0	20
31	A Survey on the Optimization of Neural Network Accelerators for Micro-AI On-Device Inference. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 532-547.	3.6	20
32	Algorithm-hardware co-design of single shot detector for fast object detection on FPGAs. , 2018, , .		19
33	A Fixed-Point Neural Network Architecture for Speech Applications on Resource Constrained Hardware. Journal of Signal Processing Systems, 2018, 90, 727-741.	2.1	18
34	Impact of Read Disturb on Multilevel RRAM based Inference Engine: Experiments and Model Prediction. , 2020, , .		18
35	FPGA-based low-batch training accelerator for modern CNNs featuring high bandwidth memory. , 2020, , .		17
36	FixyFPGA: Efficient FPGA Accelerator for Deep Neural Networks with High Element-Wise Sparsity and without External Memory Access. , 2021, , .		16

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37	Digital CMOS neuromorphic processor design featuring unsupervised online learning. , 2015, , .		15
38	K-Nearest Neighbor Hardware Accelerator Using In-Memory Computing SRAM. , 2019, , .		13
39	A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV, and SRAM PUF for Authentication and Secret Key Generation. IEEE Journal of Solid-State Circuits, 2020, 55, 2680-2690.	5.4	13
40	A 8.93-TOPS/W LSTM Recurrent Neural Network Accelerator Featuring Hierarchical Coarse-Grain Sparsity With All Parameters Stored On-Chip. IEEE Solid-State Circuits Letters, 2019, 2, 119-122.	2.0	11
41	An Energy-Efficient Deep Convolutional Neural Network Accelerator Featuring Conditional Computing and Low External Memory Access. IEEE Journal of Solid-State Circuits, 2021, 56, 803-813.	5.4	11
42	Impact of On-chip Interconnect on In-memory Acceleration of Deep Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2022, 18, 1-22.	2.3	11
43	Deep Neural Network Training Accelerator Designs in ASIC and FPGA. , 2020, , .		11
44	Neuromorphic Hardware Accelerator for SNN Inference based on STT-RAM Crossbar Arrays. , 2019, , .		9
45	Inference engine benchmarking across technological platforms from CMOS to RRAM. , 2019, , .		9
46	Modeling and Optimization of SRAM-based In-Memory Computing Hardware Design. , 2021, , .		9
47	Impact of Multilevel Retention Characteristics on RRAM based DNN Inference Engine. , 2021, , .		9
48	Ranking the parameters of deep neural networks using the fisher information. , 2016, , .		7
49	A Parallel RRAM Synaptic Array Architecture for Energy-Efficient Recurrent Neural Networks. , 2018, , .		6
50	A 8.93-TOPS/W LSTM Recurrent Neural Network Accelerator Featuring Hierarchical Coarse-Grain Sparsity With All Parameters Stored On-Chip. , 2019, , .		6
51	Characterization and Mitigation of Relaxation Effects on Multi-level RRAM based In-Memory Computing. , 2021, , .		6
52	Total Ionizing Dose Effects on Multistate HfOâ‚"-Based RRAM Synaptic Array. IEEE Transactions on Nuclear Science, 2021, 68, 756-761.	2.0	6
53	Improving the accuracy and robustness of RRAM-based in-memory computing against RRAM hardware noise and adversarial attacks. Semiconductor Science and Technology, 2022, 37, 034001.	2.0	6
54	A Real-Time 17-Scale Object Detection Accelerator With Adaptive 2000-Stage Classification in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 3843-3853.	5.4	5

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55	C3SRAM: In-Memory-Computing SRAM Macro Based on Capacitive-Coupling Computing. , 2019, , .		5
56	Deep Convolutional Neural Network Accelerator Featuring Conditional Computing and Low External Memory Access. , 2020, , .		5
57	XST: A Crossbar Column-wise Sparse Training for Efficient Continual Learning. , 2022, , .		5
58	Leveraging Noise and Aggressive Quantization of In-Memory Computing for Robust DNN Hardware Against Adversarial Input and Weight Attacks. , 2021, , .		4
59	Improving DNN Hardware Accuracy by In-Memory Computing Noise Injection. IEEE Design and Test, 2022, 39, 71-80.	1.2	4
60	Fully-integrated switched-capacitor voltage regulator with on-chip current-sensing and workload optimization in 32nm SOI CMOS. , 2015, , .		3
61	Reducing the Model Order of Deep Neural Networks Using Information Theory. , 2016, , .		3
62	An On-Chip Learning Accelerator for Spiking Neural Networks using STT-RAM Crossbar Arrays. , 2020, , .		3
63	Peripheral Circuit Design Considerations of Neuro-inspired Architectures. , 2017, , 167-182.		3
64	A Smart Hardware Security Engine Combining Entropy Sources of ECG, HRV and SRAM PUF for Authentication and Secret Key Generation. , 2019, , .		3
65	System-Level Benchmarking of Chiplet-based IMC Architectures for Deep Neural Network Acceleration. , 2021, , .		3
66	Flying and decoupling capacitance optimization for area-constrained on-chip switched-capacitor voltage regulators. , 2017, , .		2
67	Well-Posed Verilog-A Compact Model for Phase Change Memory. , 2018, , .		2
68	Custom Sub-Systems and Circuits for Deep Learning: Guest Editorial Overview. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2019, 9, 247-252.	3.6	2
69	Regulation Control Design Techniques for Integrated Switched Capacitor Voltage Regulators. , 2020, , .		1
70	Online Knowledge Acquisition with the Selective Inherited Model. , 2020, , .		1
71	XBM: A Crossbar Column-wise Binary Mask Learning Method for Efficient Multiple Task Adaption. , 2022, , .		1
72	Sparse and Robust RRAM-based Efficient In-memory Computing for DNN Inference. , 2022, , .		1

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73	A real-time 17-scale object detection accelerator with adaptive 2000-stage classification in 65nm CMOS. , 2017, , .		0
74	Process Scalability of Pulse-Based Circuits for Analog Image Convolution. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 2929-2938.	5.4	0
75	Guest Editorial Low-Power, Adaptive Neuromorphic Systems: Devices, Circuit, Architectures and Algorithms. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 1-5.	3.6	0
76	Hybrid In-Memory Computing Architecture for the Training of Deep Neural Networks. , 2021, , .		0
77	Guest Editorial Cross-Layer Designs, Methodologies, and Systems to Enable Micro AI for On-Device Intelligence. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 527-531.	3.6	0