Congyin Shi

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/4562890/publications.pdf

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23	346	1163117 8	1474206 9
papers	citations	h-index	g-index

23	23	23	374
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Highly Power-Efficient Active-RC Filters With Wide Bandwidth-Range Using Low-Gain Push-Pull Opamps. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 95-107.	5.4	70
2	Unipolar $hbox{TaO}_{x}$-Based Resistive Change Memory Realized With Electrode Engineering. IEEE Electron Device Letters, 2010, 31, 966-968.	3.9	57
3	A Single-Chip CMOS UHF RFID Reader Transceiver for Chinese Mobile Applications. IEEE Journal of Solid-State Circuits, 2010, 45, 1316-1329.	5.4	56
4	Thwarting analog IC piracy via combinational locking. , 2017, , .		38
5	150â€“850 MHz High-Linearity Sine-wave Synthesizer Architecture Based on FIR Filter Approach and SFDR Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2227-2237.	5.4	30
6	A Built-In Self-Test and <italic>In Situ</italic> Analog Circuit Optimization Platform. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3445-3458.	5.4	24
7	On-Chip Two-Tone Synthesizer Based on a Mixing-FIR Architecture. IEEE Journal of Solid-State Circuits, 2017, 52, 2105-2116.	5.4	17
8	A 4.2 mm^{2} 72 mW Multistandard Direct-Conversion DTV Tuner in 65 nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 280-292.	5.4	12
9	Built-In Self Optimization for Variation Resilience of Analog Filters. , 2015, , .		9
10	Forming-Less Unipolar TaOx-Based RRAM with Large CC-Independence Range for High Density Memory Applications. ECS Transactions, 2010, 27, 3-8.	0.5	8
11	A 2.3mA 240-to-500MHz 6. , 2010, , .		6
12	Thermally stable TaO<inf>x</inf>-based resistive memory with TiN electrode for MLC application. , 2010, , .		4
13	A 31mA CMOS wideband BD-II B2. , 2010, , .		4
14	−99dBc/Hz@10kHz 1MHz-step dual-loop integer-N PLL with anti-mislocking frequency calibration for global navigation satellite system receiver. , 2011, , .		4
15	A dual loop dual VCO CMOS PLL using a novel coarse tuning technique for DTV. , 2008, , .		2
16	1mW 4-5GHz packaged VCO with bonding-to-ground inductors. , 2010, , .		2
17	A 0.47mW 6th-order 20MHz active filter using highly power-efficient Opamp. , 2011, , .		2
18	An On-Chip Built-in Linearity Estimation Methodology and Hardware Implementation. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 897-908.	5.4	1

#	Article	IF	Citations
19	A single-chip CMOS UHF RFID Reader transceiver for mobile applications. , 2009, , .		0
20	A W-band divider-less cascading frequency synthesizer with push-push ×4 frequency multiplier and sampling PLL in 65nm CMOS. , 2012, , .		0
21	A 65 mW fully integrated UHF-band CMMB tuner in 65 nm CMOS process. Science China Information Sciences, 2013, 56, 1-5.	4.3	0
22	A low power and low in-band phase noise W-band frequency synthesizer in 65 nm CMOS. Microwave and Optical Technology Letters, 2014, 56, 2014-2018.	1.4	0
23	A Time-Domain Digital-Intensive Built-In Tester for Analog Circuits. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 313-320.	1.2	0