Jeffrey Kauppila

List of Publications by Year
in descending order

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52	884	16	27
papers	citations	h-index	g-index

516710 526287

52	52	52	782
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	<i>In Situ</i> Measurement of TID-Induced Leakage Using On-Chip Frequency Modulation. IEEE Transactions on Nuclear Science, 2022, 69, 367-373.	2.0	1
2	Mitigating Total-Ionizing-Dose-Induced Threshold-Voltage Shifts Using Back-Gate Biasing in 22-nm FD-SOI Transistors. IEEE Transactions on Nuclear Science, 2022, 69, 374-380.	2.0	6
3	Modeling COTS System TID Response With Monte Carlo Sampling and Transistor Swapping Experiments. IEEE Transactions on Nuclear Science, 2021, 68, 1008-1013.	2.0	0
4	Single-Event Upsets in a 7-nm Bulk FinFET Technology With Analysis of Threshold Voltage Dependence. IEEE Transactions on Nuclear Science, 2021, 68, 823-829.	2.0	11
5	Single-Event Latchup in a 7-nm Bulk FinFET Technology. IEEE Transactions on Nuclear Science, 2021, 68, 830-834.	2.0	13
6	A System-Level Modeling Approach for Simulating Radiation Effects in Successive-Approximation Analog-to-Digital Converters. IEEE Transactions on Nuclear Science, 2021, 68, 1465-1472.	2.0	2
7	Radiation Hardened by Design Subsampling Phase-Locked Loop Techniques in PD-SOI. IEEE Transactions on Nuclear Science, 2020, 67, 1144-1151.	2.0	7
8	Exploiting SEU Data Analysis to Extract Fast SET Pulses. IEEE Transactions on Nuclear Science, 2019, 66, 932-937.	2.0	1
9	Empirical Modeling of FinFET SEU Cross Sections Across Supply Voltage. IEEE Transactions on Nuclear Science, 2019, 66, 1427-1432.	2.0	8
10	A Bias-Dependent Single-Event-Enabled Compact Model for Bulk FinFET Technologies. IEEE Transactions on Nuclear Science, 2019, 66, 635-642.	2.0	9
11	Frequency Dependence of Heavy-Ion-Induced Single-Event Responses of Flip-Flops in a 16-nm Bulk FinFET Technology. IEEE Transactions on Nuclear Science, 2018, 65, 413-417.	2.0	9
12	Angular Effects on Single-Event Mechanisms in Bulk FinFET Technologies. IEEE Transactions on Nuclear Science, 2018, 65, 223-230.	2.0	24
13	Impact of Single-Event Transient Duration and Electrical Delay at Reduced Supply Voltages on SET Mitigation Techniques. IEEE Transactions on Nuclear Science, 2018, 65, 362-368.	2.0	14
14	An Empirical Model for Predicting SE Cross Section for Combinational Logic Circuits in Advanced Technologies. IEEE Transactions on Nuclear Science, 2018, 65, 304-310.	2.0	7
15	Exploiting Parallelism and Heterogeneity in a Radiation Effects Test Vehicle for Efficient Single-Event Characterization of Nanoscale Circuits. IEEE Transactions on Nuclear Science, 2018, 65, 486-494.	2.0	13
16	Time-Domain Modeling of All-Digital PLLs to Single-Event Upset Perturbations. IEEE Transactions on Nuclear Science, 2018, 65, 311-317.	2.0	3
17	The Impact of Charge Collection Volume and Parasitic Capacitance on SEUs in SOI- and Bulk-FinFET D Flip-Flops. IEEE Transactions on Nuclear Science, 2018, 65, 326-330.	2.0	20
18	Effects of Total-Ionizing-Dose Irradiation on Single-Event Response for Flip-Flop Designs at a 14-/16-nm Bulk FinFET Technology Node. IEEE Transactions on Nuclear Science, 2018, 65, 1928-1934.	2.0	7

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19	Power-Aware SE Analysis of Different FF Designs at the 14-/16-nm Bulk FinFET CMOS Technology Node. IEEE Transactions on Nuclear Science, 2018, 65, 1866-1871.	2.0	3
20	Dual-Interlocked Logic for Single-Event Transient Mitigation. IEEE Transactions on Nuclear Science, 2018, 65, 1872-1878.	2.0	13
21	Effect of Transistor Variants on Single-Event Transients at the 14-/16-nm Bulk FinFET Technology Generation. IEEE Transactions on Nuclear Science, 2018, 65, 1807-1813.	2.0	16
22	Estimating Single-Event Logic Cross Sections in Advanced Technologies. IEEE Transactions on Nuclear Science, 2017, , 1-1.	2.0	17
23	Analysis of TID Process, Geometry, and Bias Condition Dependence in 14-nm FinFETs and Implications for RF and SRAM Performance. IEEE Transactions on Nuclear Science, 2017, 64, 285-292.	2.0	55
24	Analysis of Bulk FinFET Structural Effects on Single-Event Cross Sections. IEEE Transactions on Nuclear Science, 2017, 64, 441-448.	2.0	45
25	Advanced node-splitting techniques for radiation-hardened analog/mixed-signal circuits. , 2016, , .		2
26	Estimation of single-event transient pulse characteristics for predictive analysis. , 2016, , .		4
27	An Area Efficient Stacked Latch Design Tolerant to SEU in 28 nm FDSOI Technology. IEEE Transactions on Nuclear Science, 2016, 63, 3003-3009.	2.0	21
28	Temperature dependence of soft-error rates for FF designs in 20-nm bulk planar and 16-nm bulk FinFET technologies. , 2016, , .		24
29	A Comparison of the SEU Response of Planar and FinFET D Flip-Flops at Advanced Technology Nodes. IEEE Transactions on Nuclear Science, 2016, 63, 266-272.	2.0	54
30	Estimation of Single-Event-Induced Collected Charge for Multiple Transistors Using Analytical Expressions. IEEE Transactions on Nuclear Science, 2015, 62, 2853-2859.	2.0	3
31	Proton Irradiation as a Screen for Displacement-Damage Sensitivity in Bipolar Junction Transistors. IEEE Transactions on Nuclear Science, 2015, 62, 2498-2504.	2.0	8
32	Single-Event Upset Characterization Across Temperature and Supply Voltage for a 20-nm Bulk Planar CMOS Technology. IEEE Transactions on Nuclear Science, 2015, 62, 2613-2619.	2.0	19
33	Heavy-Ion Induced SETs in 32nm SOI Inverter Chains. , 2015, , .		3
34	Geometry-Aware Single-Event Enabled Compact Models for Sub-50Ânm Partially Depleted Silicon-on-Insulator Technologies. IEEE Transactions on Nuclear Science, 2015, 62, 1589-1598.	2.0	17
35	Irradiation and Temperature Effects for a 32Ânm RF Silicon-on-Insulator CMOS Process. IEEE Transactions on Nuclear Science, 2014, 61, 3037-3042.	2.0	8
36	RHBD Technique for Single-Event Charge Cancellation in Folded-Cascode Amplifiers. IEEE Transactions on Nuclear Science, 2013, 60, 2756-2761.	2.0	12

#	Article	IF	Citations
37	The Quad-Path Hardening Technique for Switched-Capacitor Circuits. IEEE Transactions on Nuclear Science, 2013, 60, 4356-4361.	2.0	5
38	Effect of Device Variants in 32Ânm and 45Ânm SOI on SET Pulse Distributions. IEEE Transactions on Nuclear Science, 2013, 60, 4399-4404.	2.0	21
39	Sensitivity of High-Frequency RF Circuits to Total Ionizing Dose Degradation. IEEE Transactions on Nuclear Science, 2013, 60, 4498-4504.	2.0	20
40	Effect of threshold voltage implants on single-event error rates of D flip-flops in 28-nm bulk CMOS. , 2013, , .		10
41	On-Chip Measurement of Single-Event Transients in a 45 nm Silicon-on-Insulator Technology. IEEE Transactions on Nuclear Science, 2012, 59, 2748-2755.	2.0	44
42	Single-Event-Hardened CMOS Operational Amplifier Design. IEEE Transactions on Nuclear Science, 2012, 59, 803-810.	2.0	22
43	Effect of Negative Bias Temperature Instability on the Single Event Upset Response of 40 nm Flip-Flops. IEEE Transactions on Nuclear Science, 2012, 59, 2651-2657.	2.0	14
44	A Hysteresis-Based D-Flip-Flop Design in 28 nm CMOS for Improved SER Hardness at Low Performance Overhead. IEEE Transactions on Nuclear Science, 2012, 59, 2847-2851.	2.0	14
45	Differential Charge Cancellation (DCC) Layout as an RHBD Technique for Bulk CMOS Differential Circuit Design. IEEE Transactions on Nuclear Science, 2012, 59, 2867-2871.	2.0	18
46	A single-event-hardened CMOS operational amplifier design. , 2011, , .		1
47	RHBD Bias Circuits Utilizing Sensitive Node Active Charge Cancellation. IEEE Transactions on Nuclear Science, 2011, 58, 3060-3066.	2.0	16
48	Impact of Process Variations on SRAM Single Event Upsets. IEEE Transactions on Nuclear Science, 2011, 58, 834-839.	2.0	30
49	Circuit-Level Layout-Aware Single-Event Sensitive-Area Analysis of 40-nm Bulk CMOS Flip-Flops Using Compact Modeling. IEEE Transactions on Nuclear Science, 2011, 58, 2680-2686.	2.0	24
50	Radiation hardness of FDSOI and FinFET technologies. , 2011, , .		28
51	A Bias-Dependent Single-Event Compact Model Implemented Into BSIM4 and a 90 nm CMOS Process Design Kit. IEEE Transactions on Nuclear Science, 2009, 56, 3152-3157.	2.0	131
52	Probabilistic Evaluation of Analog Single Event Transients. IEEE Transactions on Nuclear Science, 2007, 54, 2131-2136.	2.0	7