

Yingtao Ding

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Ultra-Deep Annular Cu Through-Silicon-Vias Fabricated Using Single-Sided Process. IEEE Electron Device Letters, 2022, 43, 426-429.	3.9	4
2	Coprime Nested Arrays for DOA Estimation: Exploiting the Nesting Property of Coprime Array. IEEE Signal Processing Letters, 2022, 29, 444-448.	3.6	19
3	Recent progress in metasurface-enabled optical waveplates. Nanophotonics, 2022, 11, 2219-2244.	6.0	39
4	Programmable van der Waals heterostructure-enabled optoelectronic synaptic floating-gate transistors with ultra-low energy consumption. Information Materials, 2022, 4, .	17.3	58
5	Stiffness-Tunable Microstructures Based on Electrothermal Bimorph Beams. , 2021, , .		0
6	Optically stimulated synaptic transistor based on MoS ₂ /quantum dots mixed-dimensional heterostructure with gate-tunable plasticity. Optics Letters, 2021, 46, 1748.	3.3	12
7	Optogenetics-inspired Neuromorphic Optoelectronic Synaptic Transistors with Optically Modulated Plasticity. Advanced Optical Materials, 2021, 9, 2002232.	7.3	28
8	Dual-Functional Optical Waveplates Based on Gap Surface Plasmon Metasurfaces. Advanced Optical Materials, 2021, 9, 2002253.	7.3	21
9	Development of Cu Seed Layers in Ultra-High Aspect Ratio Through-Silicon-Vias (TSVs) with Small Diameters. , 2021, , .		3
10	An All-Wet, Low Cost RDL Fabrication Process with Electroless Plated Seed/Barrier Layers. , 2021, , .		2
11	Study on atomic migration of copper through-silicon-vias with Bosch scallops. Microelectronics Reliability, 2021, 123, 114178.	1.7	6
12	Mixed-Dimensional Van der Waals Heterostructures Enabled Optoelectronic Synaptic Devices for Neuromorphic Applications. Advanced Functional Materials, 2021, 31, 2105625.	14.9	39
13	Enabling Continuous Cu Seed Layer for Deep Through-Silicon-Vias With High Aspect Ratio by Sequential Sputtering and Electroless Plating. IEEE Electron Device Letters, 2021, 42, 1520-1523.	3.9	10
14	Flexible Broadband Photodetectors Enabled by MXene/PbS Quantum Dots Hybrid Structure. IEEE Electron Device Letters, 2021, 42, 1814-1817.	3.9	12
15	A Low-Cost and Low-Temperature Method to Realize Carbon Nanotube Conductor in Through-Silicon-Via. , 2021, , .		0
16	Phase-change metasurface for switchable vector vortex beam generation. Optics Express, 2021, 29, 42762.	3.4	13
17	Paper-based flexible broadband photodetectors functionalized by PbS quantum dots/Carbon nanotube networks hybrid structure. , 2021, , .		0
18	MEMS Ultrasound Transducers for Endoscopic Photoacoustic Imaging Applications. Micromachines, 2020, 11, 928.	2.9	30

#	ARTICLE	IF	CITATIONS
19	Extended Transformed Nested Arrays for DOA Estimation of Non-Circular Sources. IEEE Access, 2020, 8, 162350-162362.	4.2	11
20	A Novel Silicon-Air-Silicon Through-Silicon-Via Structure Realized Using Double-Side Partially Overlapping Etching. IEEE Electron Device Letters, 2020, 41, 1544-1547.	3.9	5
21	Coupled Thermo-Mechanical Analysis of 3D ICs Based on an Equivalent Modeling Methodology With Sub-Modeling. IEEE Access, 2020, 8, 14146-14154.	4.2	9
22	A Low-Voltage, Low-Current, Digital-Driven MEMS Mirror for Low-Power LiDAR. , 2020, 4, 1-4.		16
23	A Fully Integrated K-Band Dual Down-Conversion Receiver for Radar Applications in 90 nm CMOS. IEEE Access, 2020, 8, 19576-19589.	4.2	2
24	Analog-controlled light microshutters based on electrothermal actuation for smart windows. Optics Express, 2020, 28, 33106.	3.4	8
25	Comparative evaluations on scallop-induced electric-thermo-mechanical reliability of through-silicon-vias. Microelectronics Reliability, 2019, 103, 113512.	1.7	14
26	A Compact Omnidirectional Laser Scanner Based on an Electrothermal Tripod Mems Mirror for Lidar Please Leave. , 2019, , .		8
27	A Piezoelectric MEMS Loud Speaker Based on Ceramic PZT. , 2019, , .		7
28	A 25â€“35 GHz 5-bit digital attenuator with low RMS amplitude error and low phase variation in 65 nm CMOS. IEICE Electronics Express, 2019, 16, 20190394-20190394.	0.8	1
29	Development of Eccentric Spin Coating of Polymer Liner for Low-Temperature TSV Technology With Ultra-Fine Diameter. IEEE Electron Device Letters, 2019, 40, 95-98.	3.9	14
30	Design and Evaluation of a Novel and Ultra-Compact Fully-TGV-based Self-Shielding Bandpass Filter for 5G Applications. , 2019, , .		3
31	A Novel Nested Configuration Based on the Difference and Sum Co-Array Concept. Sensors, 2018, 18, 2988.	3.8	25
32	Sampling and Reconstruction of Multiband Signals in Multiresolution Subspaces Associated with the Fractional Wavelet Transform. IEEE Signal Processing Letters, 2018, , 1-1.	3.6	3
33	A Novel Noncircular MUSIC Algorithm Based on the Concept of the Difference and Sum Coarray. Sensors, 2018, 18, 344.	3.8	35
34	Elimination of Scallop-Induced Stress Fluctuation on Through-Silicon-Vias (TSVs) by Employing Polyimide Liner. IEEE Transactions on Device and Materials Reliability, 2018, 18, 266-272.	2.0	10
35	Impact of polyimide liner on high-aspect-ratio through-silicon-vias (TSVs): electrical characteristics and copper protrusion. Microsystem Technologies, 2017, 23, 3757-3764.	2.0	3
36	Investigation of dynamic thermal behaviors of an electrothermal micromirror. Sensors and Actuators A: Physical, 2017, 263, 269-275.	4.1	7

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37	Modelling and Experimental Verification of Step Response Overshoot Removal in Electrothermally-Actuated MEMS Mirrors. <i>Micromachines</i> , 2017, 8, 289.	2.9	12
38	Electrical characteristics and thermal reliability of blind through-silicon-vias with polyimide liners. , 2016, , .		4
39	Electrical Characterization of Coaxial Silicon-Insulator-Silicon Through-Silicon Vias: Theoretical Analysis and Experiments. <i>IEEE Transactions on Electron Devices</i> , 2016, 63, 4880-4887.	3.0	19
40	An analytical model for capacitance of silicon-insulator-silicon through-silicon-vias. , 2016, , .		0
41	Low capacitance and highly reliable blind through-silicon-vias (TSVs) with vacuum-assisted spin coating of polyimide dielectric liners. <i>Science China Technological Sciences</i> , 2016, 59, 1581-1590.	4.0	9
42	A large-piston scanning electrothermal micromirror with a temperature control frame. , 2016, , .		1
43	Low cost polyimide liner formation with vacuum-assisted spin coating for through-silicon-vias. , 2016, , .		3
44	Wideband Capacitance Evaluation of Silicon-Insulator-Silicon Through-Silicon-Vias for 3D Integration Applications. <i>IEEE Electron Device Letters</i> , 2016, 37, 216-219.	3.9	14
45	Highly conformal polyimide liner deposition in high-aspect-ratio through silicon vias. <i>Micro and Nano Letters</i> , 2016, 11, 253-255.	1.3	5
46	Study of Vacuum-Assisted Spin Coating of Polymer Liner for High-Aspect-Ratio Through-Silicon-Via Applications. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2016, 6, 501-509.	2.5	12
47	Innovative polyimide liner deposition method for high-aspect-ratio and high-density through-silicon-vias (TSVs). <i>Microelectronic Engineering</i> , 2016, 149, 78-84.	2.4	12
48	Design of a dynamically reconfigurable arithmetic unit for matrix algorithms. , 2015, , .		0
49	An Efficient Algorithm for Direction Finding against Unknown Mutual Coupling. <i>Sensors</i> , 2014, 14, 20064-20077.	3.8	11
50	Investigation on mechanism of polymer filling in high-aspect-ratio trenches for through-silicon-via (TSV) application. <i>Science China Technological Sciences</i> , 2014, 57, 1616-1625.	4.0	12
51	Thermal reliability analysis and optimization of polymer insulating through-silicon-vias (TSVs) for 3D integration. <i>Science China Technological Sciences</i> , 2014, 57, 128-135.	4.0	7
52	Cell trapping and patterning using dielectric-structure-assisted negative dielectrophoresis. <i>Science China Technological Sciences</i> , 2013, 56, 1001-1007.	4.0	2
53	Anisotropic electrical properties of aligned PtSe ₂ nanoribbon arrays grown by a pre-patterned selective selenization process. <i>Nano Research</i> , 0, , 1.	10.4	1