Gerald E Sobelman

List of Publications by Year
in descending order

68	488	687220 13	752573 20
papers	citations	h-index	g-index

68	68	68	454
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Architectures for multi-gigabit wire-linked clock and data recovery. IEEE Circuits and Systems Magazine, 2008, 8, 45-57.	2.6	61
2	A Reduced-Complexity Architecture for LDPC Layered Decoding Schemes. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1099-1103.	2.1	40
3	Stochastic MIMO Detector Based on the Markov Chain Monte Carlo Algorithm. IEEE Transactions on Signal Processing, 2014, 62, 1454-1463.	3.2	29
4	An Intra-Iterative Interference Cancellation Detector for Large-Scale MIMO Communications Based on Convex Optimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 2062-2072.	3.5	27
5	Hybrid Beamforming/Combining for Millimeter Wave MIMO: A Machine Learning Approach. IEEE Transactions on Vehicular Technology, 2020, 69, 11353-11368.	3.9	25
6	Sparse Code Multiple Access Decoding Based on a Monte Carlo Markov Chain Method. IEEE Signal Processing Letters, 2016, 23, 639-643.	2.1	23
7	Generic Mixed-Radix FFT Pruning. IEEE Signal Processing Letters, 2012, 19, 167-170.	2.1	21
8	Asymptotic estimates and borel resummation for a doubly anharmonic oscillator. Physical Review D, 1979, 19, 3754-3767.	1.6	20
9	FPGA-based digit-serial CSD FIR filter for image signal format conversion. Microelectronics Journal, 2002, 33, 501-508.	1.1	19
10	Stochastic Iterative MIMO Detection System: Algorithm and Hardware Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1205-1214.	3.5	19
11	New XOR/XNOR and full adder circuits for low voltage, low power applications. Microelectronics Journal, 1998, 29, 509-517.	1.1	16
12	Performance evaluation and optimal design for FPGA-based digit-serial DSP functions. Computers and Electrical Engineering, 2003, 29, 357-377.	3.0	16
13	PLL performance comparison with application to spread spectrum clock generator design. Analog Integrated Circuits and Signal Processing, 2010, 63, 197-216.	0.9	14
14	Mesh-star Hybrid NoC architecture with CDMA switch. , 2009, , .		12
15	Sparse LMS with segment zero attractors for adaptive estimation of sparse signals. , 2010, , .		10
16	Flexible LDPC decoder architecture for high-throughput applications. , 2008, , .		9
17	Gradient-based target localization in robotic sensor networks. Pervasive and Mobile Computing, 2009, 5, 37-48.	2.1	9
18	Bus Energy Consumption for Multilevel Signals. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 64-71.	3.5	9

#	Article	IF	Citations
19	Hardware Efficient Massive MIMO Detector Based on the Monte Carlo Tree Search Method. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2017, 7, 523-533.	2.7	8
20	Low-Power Bus Transform Coding for Multilevel Signals. , 2006, , .		7
21	Adaptive quantization in min-sum based irregular LDPC decoder. , 2008, , .		7
22	MIMO Transceiver Design Based on a Modified Geometric Mean Decomposition. , 2007, , .		6
23	A comparative study of glitch-free true single-phase clocked D flip-flop circuits at low supply voltage. Microelectronics Journal, 1998, 29, 1025-1031.	1.1	5
24	Optimality of Bus-Invert Coding. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1134-1138.	2.2	5
25	Cscan: A Correlation-based Scheduling Algorithm for Wireless Sensor Networks. , 2008, , .		5
26	Scaling, Offset, and Balancing Techniques in FFT-Based BP Nonbinary LDPC Decoders. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 277-281.	2.2	5
27	Iterative Computation of FIR MIMO MMSE-DFE With Flexible Complexity-Performance Tradeoff. IEEE Transactions on Signal Processing, 2013, 61, 2394-2404.	3.2	5
28	A low complexity SCMA detector based on stochastic computation. , 2017, , .		5
29	FPGA-Based Design of a Pulsed-OFDM System. , 2006, , .		4
30	Sparseness-Controlled Adaptive Tap algorithms for partial update adaptive filters. , 2009, , .		4
31	Strong-coupling expansions for multidimensional Ising andO(n)spin systems. Physical Review B, 1981, 24, 1493-1499.	1.1	3
32	Reconfigurable baseband processing platform for communication systems. , 2008, , .		3
33	A low complexity floating-point complex multiplier with a three-term dot-product unit. , 2014, , .		3
34	Improved design of digital 1-D and 2-D notch filters using general feedback structure. , 2016, , .		3
35	An Efficient CNN Accelerator for Low-Cost Edge Systems. Transactions on Embedded Computing Systems, 2022, 21, 1-20.	2.1	3
36	Bandwidth-reusable CDMA NoC with flexible codeword assignment. , 2007, , .		2

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37	A heterogeneous reconfigurable baseband architecture for wireless LAN transceivers. , 2008, , .		2
38	Software Defined Radio architecture using a multicasting Network-on-Chip. , 2009, , .		2
39	FFT implementation with Multi-operand floating point units. , 2011, , .		2
40	Wideband spectrum sensing using the all-phase FFT. , 2011, , .		2
41	A novel fixed-complexity soft-output MIMO detector using parallel bidirectional scheme. , 2013, , .		2
42	Stochastic computing implementation of trigonometric and hyperbolic functions. , 2017, , .		2
43	Memory Segment Matching Network Based Image Geo-Localization. IEEE Access, 2019, 7, 77448-77459.	2.6	2
44	Cluster Partitioning Techniques for Data Path Synthesis. VLSI Design, 1994, 1, 181-192.	0.5	1
45	SPC08-5: Noise Model Analysis of Optimized Mixed-Radix Structures for Pulsed OFDM. IEEE Global Telecommunications Conference (GLOBECOM), 2006, , .	0.0	1
46	An Efficient Multi-protocol RFID Interrogator Baseband Processor based on a Reconfigurable Architecture. , 2008, , .		1
47	Semi-distributed scheduling for flexible codeword assignment in a CDMA Network-on-Chip. , 2009, , .		1
48	Reed-Solomon Codec for a Reconfigurable Baseband Processing Platform. , 2009, , .		1
49	Frequency domain adaptive tap partial update adaptive algorithm for network echo cancellation. , 2010, , .		1
50	QoS-Constrained MIMO Subchannel Allocation in SDR Using the Tunable Channel Decomposition. , 2010, , .		1
51	General lattice wave digital filter with phase compensation scheme. , 2011, , .		1
52	A novel hardware-oriented decoding algorithm for non-binary LDPC codes. , 2012, , .		1
53	Low complexity state metric compression technique in turbo decoder. IEICE Electronics Express, 2013, 10, 20130485-20130485.	0.3	1
54	A database-driven Ant Colony Algorithm for PLC networking. IEICE Electronics Express, 2014, 11, 20140957-20140957.	0.3	1

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55	A low-complexity FFT Processor using two-dimensional algebraic integer encoding. , 2016, , .		1
56	Switch-level Differential Fault Simulation of MOS VLSI Circuits. VLSI Design, 1996, 4, 217-229.	0.5	0
57	VLSI DESIGN OF DIGIT-SERIAL FPGA ARCHITECTURE. Journal of Circuits, Systems and Computers, 2004, 13, 17-52.	1.0	0
58	Multi-level signaling for energy-efficient on-chip interconnects. , 2007, , .		0
59	High Speed Look-Ahead LMS Detector for MIMO Systems. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	0
60	Reconfigurable MIMO transceiver design using the tunable channel decomposition. , 2010, , .		0
61	Memory size reduction for LDPC layered decoders. , 2010, , .		0
62	Novel and flexible Complex Coefficient Linear phase IIR filters for communications. , 2010, , .		0
63	A high-throughput LDPC decoder architecture for high-rate WPAN systems. , 2011, , .		0
64	Network-coding-based distributed relay scheme for PLC networks. , 2015, , .		0
65	A low complexity algorithm and architecture for MIMO detection without QR decomposition. , 2015, , .		0
66	Reduced complexity look-up table based ï€-rotation LDPC decoder. , 2016, , .		0
67	An SVA hardware monitor with off-line replay. , 2016, , .		0
68	Implementations of FFT and STBD for MIMO-OFDM on a Reconfigurable Baseband Platform. IEICE Transactions on Information and Systems, 2010, E93-D, 811-821.	0.4	0