Anni Lu

List of Publications by Year
in descending order

		1307594	1372567
14 papers	**314** citations	**7** h-index	**10** g-index
14 all docs	**14** docs citations	**14** times ranked	**187** citing authors

#	Article	IF	Citations
1	Robust Processing-In-Memory With Multibit ReRAM Using Hessian-Driven Mixed-Precision Computation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1006-1019.	2.7	7
2	Design and Optimization of Non-Volatile Capacitive Crossbar Array for In-Memory Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 784-788.	3.0	5
3	3D AND-Type Ferroelectric Transistors for Compute-in-Memory and the Variability Analysis. IEEE Electron Device Letters, 2022, 43, 304-307.	3.9	15
4	Nonvolatile Capacitive Crossbar Array for Inâ€Memory Computing. Advanced Intelligent Systems, 2022, 4, .	6.1	16
5	An Algorithm-Hardware Co-Design for Bayesian Neural Network Utilizing SOT-MRAMâ€™s Inherent Stochasticity. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2022, 8, 27-34.	1.5	4
6	Compute-in-Memory Chips for Deep Learning: Recent Trends and Prospects. IEEE Circuits and Systems Magazine, 2021, 21, 31-56.	2.3	115
7	A Runtime Reconfigurable Design of Compute-in-Memory based Hardware Accelerator. , 2021, , .		3
8	Design of Non-volatile Capacitive Crossbar Array for In-Memory Computing. , 2021, , .		8
9	Compute-in-RRAM with Limited On-chip Resources. , 2021, , .		1
10	NeuroSim Simulator for Compute-in-Memory Hardware Accelerator: Validation and Benchmark. Frontiers in Artificial Intelligence, 2021, 4, 659060.	3.4	23
11	DNN+NeuroSim V2.0: An End-to-End Benchmarking Framework for Compute-in-Memory Accelerators for On-Chip Training. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2306-2319.	2.7	96
12	Compute-in-Memory: From Device Innovation to 3D System Integration. , 2021, , .		5
13	Genetic Algorithm-Based Energy-Aware CNN Quantization for Processing-In-Memory Architecture. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 649-662.	3.6	5
14	Benchmark of the Compute-in-Memory-Based DNN Accelerator With Area Constraint. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1945-1952.	3.1	11