Takahiro Hanyu

List of Publications by Year
in descending order

56	1,813	567144 15	345118 36
papers	citations	h-index	g-index

56	56	56	1390
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	CMOS Invertible Logic: Bidirectional operation based on the probabilistic device model and stochastic computing. IEEE Nanotechnology Magazine, 2022, 16, 33-46.	0.9	4
2	A Design Framework for Invertible Logic. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 655-665.	1.9	13
3	Multi-Context TCAM-Based Selective Computing: Design Space Exploration for a Low-Power NN. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 67-76.	3.5	9
4	Design framework for an energy-efficient binary convolutional neural network accelerator based on nonvolatile logic. Nonlinear Theory and Its Applications IEICE, 2021, 12, 695-710.	0.4	2
5	Design of a highly reliable nonvolatile flip-flop incorporating a common-mode write error detection capability. Japanese Journal of Applied Physics, 2021, 60, SBBB02.	0.8	2
6	Design of an energy-efficient binarized convolutional neural network accelerator using a nonvolatile field-programmable gate array with only-once-write shifting. Japanese Journal of Applied Physics, 2021, 60, SBBB07.	0.8	3
7	High Convergence Rates of CMOS Invertible Logic Circuits Based on Many-Body Hamiltonians. , 2021, , .		3
8	Nonvolatile Field-Programmable Gate Array Using a Standard-Cell-Based Design Flow. IEICE Transactions on Information and Systems, 2021, E104.D, 1111-1120.	0.4	0
9	Scalable Hardware Architecture for Invertible Logic with Sparse Hamiltonian Matrices. , 2021, , .		2
10	A Memory-Access-Minimized BCNN Accelerator Using Nonvolatile FPGA with Only-Once- Write Shifting. , 2021, , .		0
11	In-Hardware Training Chip Based on CMOS Invertible Logic for Machine Learning. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1541-1550.	3.5	19
12	Memristive Computational Memory Using Memristor Overwrite Logic (MOL). IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2370-2382.	2.1	16
13	Design of a cost-efficient controller for realizing a data-shift-minimized nonvolatile field-programmable gate array. Japanese Journal of Applied Physics, 2020, 59, SGGB13.	0.8	1
14	Impact of MTJ-based nonvolatile circuit techniques for energy-efficient binary neural network hardware. Japanese Journal of Applied Physics, 2020, 59, 050602.	0.8	6
15	Prospects of Edge AI Hardware Using Nonvolatile Logic. Ieice Ess Fundamentals Review, 2020, 13, 269-276.	0.1	0
16	Design and Evaluation of a Synthesizable Standard-Cell-Based Nonvolatile FPGA. , 2020, , .		1
17	A 47.14-$muext{W}$ 200-MHz MOS/MTJ-Hybrid Nonvolatile Microcontroller Unit Embedding STT-MRAM and FPGA for IoT Applications. IEEE Journal of Solid-State Circuits, 2019, 54, 2991-3004.	3.5	39
18	Design of a highly reliable, high-speed MTJ-based lookup table circuit using fractured logic-in-memory structure. Japanese Journal of Applied Physics, 2019, 58, SBBB10.	0.8	7

#	Article	IF	Citations
19	Brain-Inspired Computing. , 2019, , 185-199.		0
20	FPGA Implementation of Binarized Perceptron Learning Hardware Using CMOS Invertible Logic. , 2019, , .		0
21	Multi-Context TCAM Based Selective Computing Architecture for a Low-Power NN. , 2019, , .		4
22	Stochastic-Computing Based Brainwave LSI Towards an Intelligence Edge. , 2019, , .		0
23	Efficient CMOS Invertible Logic Using Stochastic Computing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2263-2274.	3.5	45
24	Design of a memory-access controller with 3.71-times-enhanced energy efficiency for Internet-of-Things-oriented nonvolatile microcontroller unit. Japanese Journal of Applied Physics, 2018, 57, 04FN03.	0.8	7
25	A Generalized Stochastic Implementation of the Disparity Energy Model for Depth Perception. Journal of Signal Processing Systems, 2018, 90, 709-725.	1.4	5
26	Design of a magnetic-tunnel-junction-oriented nonvolatile lookup table circuit with write-operation-minimized data shifting. Japanese Journal of Applied Physics, 2018, 57, 04FE09.	0.8	12
27	Application of stochastic computing in brainware. Nonlinear Theory and Its Applications IEICE, 2018, 9, 406-422.	0.4	2
28	Design of MTJ-Based nonvolatile logic gates for quantized neural networks. Microelectronics Journal, 2018, 82, 13-21.	1.1	17
29	Networked Power-Gated MRAMs for Memory-Based Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2696-2708.	2.1	5
30	An Accuracy/Energy-Flexible Configurable Gabor-Filter Chip Based on Stochastic Computation With Dynamic Voltageâ€“Frequencyâ€“Length Scaling. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 444-453.	2.7	12
31	VLSI Implementation of Deep Neural Network Using Integral Stochastic Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2688-2699.	2.1	181
32	Design of a low-power nonvolatile flip-flop using three-terminal magnetic-tunnel-junction-based self-terminated mechanism. Japanese Journal of Applied Physics, 2017, 56, 04CN06.	0.8	8
33	Area/Energy-Efficient Gammatone Filters Based on Stochastic Computation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2724-2735.	2.1	15
34	Fabrication of a magnetic-tunnel-junction-based nonvolatile logic-in-memory LSI with content-aware write error masking scheme achieving 92% storage capacity and 79% power reduction. Japanese Journal of Applied Physics, 2017, 56, 04CN01.	0.8	7
35	Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing. Proceedings of the IEEE, 2016, 104, 1844-1863.	16.4	102
36	Gabor Filter Based on Stochastic Computation. IEEE Signal Processing Letters, 2015, 22, 1224-1228.	2.1	42

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37	Nonvolatile Logic-in-Memory LSI Using Cycle-Based Power Gating and its Application to Motion-Vector Prediction. IEEE Journal of Solid-State Circuits, 2015, 50, 476-489.	3.5	53
38	Cost-Efficient Self-Terminated Write Driver for Spin-Transfer-Torque RAM and Logic. IEEE Transactions on Magnetics, 2014, 50, 1-4.	1.2	53
39	A Nonvolatile Associative Memory-Based Context-Driven Search Engine Using 90 nm CMOS/MTJ-Hybrid Logic-in-Memory Architecture. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 460-474.	2.7	30
40	Design of an energy-efficient 2T-2MTJ nonvolatile TCAM based on a parallel-serial-combined search scheme. IEICE Electronics Express, 2014, 11, 20131006-20131006.	0.3	9
41	Complementary 5T-4MTJ nonvolatile TCAM cell circuit with phase-selective parallel writing scheme. IEICE Electronics Express, 2014, 11, 20140297-20140297.	0.3	7
42	Soft-error tolerant transistor/magnetic-tunnel-junction hybrid non-volatile C-element. IEICE Electronics Express, 2014, 11, 20141017-20141017.	0.3	4
43	A 1 Mb Nonvolatile Embedded Memory Using 4T2MTJ Cell With 32 b Fine-Grained Power Gating Scheme. IEEE Journal of Solid-State Circuits, 2013, 48, 1511-1520.	3.5	70
44	MTJ/MOS-hybrid logic-circuit design flow for nonvolatile logic-in-memory LSI. , 2013, , .		3
45	A 1-Mb STT-MRAM with zero-array standby power and 1.5-ns quick wake-up by 8-b fine-grained power gating. , 2013, , .		5
46	Fabrication of a magnetic tunnel junction-based 240-tile nonvolatile field-programmable gate array chip skipping wasted write operations for greedy power-reduced logic applications. IEICE Electronics Express, 2013, 10, 20130772-20130772.	0.3	22
47	Restructuring of memory hierarchy in computing system with spintronics-based technologies. , 2012, , .		27
48	Design of a 270ps-access 7-transistor/2-magnetic-tunnel-junction cell circuit for a high-speed-search nonvolatile ternary content-addressable memory. Journal of Applied Physics, 2012, 111, 07E336.	1.1	23
49	High-speed simulator including accurate MTJ models for spintronics integrated circuit design. , 2012, , .		50
50	Design of a Nine-Transistor/Two-Magnetic-Tunnel-Junction-Cell-Based Low-Energy Nonvolatile Ternary Content-Addressable Memory. Japanese Journal of Applied Physics, 2012, 51, 02BM06.	0.8	24
51	Design of a Compact Nonvolatile Four-Input Logic Element Using a Magnetic Tunnel Junction and Metalâ€“Oxideâ€“Semiconductor Hybrid Structure. Japanese Journal of Applied Physics, 2012, 51, 04DM02.	0.8	6
52	Magnetic Tunnel Junctions for Spintronic Memories and Beyond. IEEE Transactions on Electron Devices, 2007, 54, 991-1002.	1.6	460
53	Fabrication of a Nonvolatile Full Adder Based on Logic-in-Memory Architecture Using Magnetic Tunnel Junctions. Applied Physics Express, 0, 1, 091301.	1.1	302
54	Standby-Power-Free Compact Ternary Content-Addressable Memory Cell Chip Using Magnetic Tunnel Junction Devices. Applied Physics Express, 0, 2, 023004.	1.1	73

#	Article	IF	Citations
55	Beyond MRAM: Nonvolatile Logic-in-Memory VLSI. , 0, , 199-230.		1
56	Design of an active-load-localized single-ended nonvolatile lookup-table circuit for energy-efficient binary-convolutional-neural-network accelerator. Japanese Journal of Applied Physics, 0, , .	0.8	0