Stefan Wildermann

List of Publications by Year
in descending order

18	105	1937685 4	1872680 6
papers	citations	h-index	g-index

18	18	18	75
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	FAU: Fast and error-optimized approximate adder units on LUT-Based FPGAs. , 2016, , .		16
2	A LUT-Based Approximate Adder. , 2016, , .		14
3	Towards the co-evolution of industrial products and its production systems by combining models from development and hardware/software deployment in cyber-physical systems. Production Engineering, 2017, 11, 687-694.	2.3	13
4	Probabilistic Error Propagation through Approximated Boolean Networks. , 2020, , .		8
5	High-Level Synthesis for Hardware/Software Co-Design of Distributed Smart Camera Systems. , 2017, , .		7
6	Hybrid Application Mapping for Composable Many-Core Systems: Overview and Future Perspective. Journal of Low Power Electronics and Applications, 2020, 10, 38.	2.0	7
7	Secure Boot from Non-Volatile Memory for Programmable SoC Architectures. , 2020, , .		7
8	Efficient Arithmetic Error Rate Calculus for Visibility Reduced Approximate Adders. IEEE Embedded Systems Letters, 2018, 10, 37-40.	1.9	6
9	Model-Based Design Automation of Hardware/Software Co-Designs for Xilinx Zynq PSoCs. , 2018, , .		6
10	Three-Dimensional Localization of Bats: Visual and Acoustical. IEEE Sensors Journal, 2019, 19, 5825-5833.	4.7	6
11	Thermally Composable Hybrid Application Mapping for Real-Time Applications in Heterogeneous Many-Core Systems. , 2019, , .		6
12	Can Approximate Computing Reduce Power Consumption on FPGAs?. , 2018, , .		4
13	Providing Tamper-Secure SoC Updates Through Reconfigurable Hardware. Lecture Notes in Computer Science, 2021, , 242-253.	1.3	2
14	Task Migration Policy for Thermal-Aware Dynamic Performance Optimization in Many-Core Systems. IEEE Access, 2022, 10, 33787-33802.	4.2	2
15	AConFPGA: A Multiple-Output Boolean Function Approximation DSE Technique Targeting FPGAs. , 2018, , .		1
16	ReOrder: Runtime datapath generation for high-throughput multi-stream processing. , 2016, , .		0
17	Design and Evaluation of a Tunable PUF Architecture for FPGAs. ACM Transactions on Reconfigurable Technology and Systems, 2022, 15, 1-27.	2.5	0
18	Design and error analysis of accuracy-configurable sequential multipliers via segmented carry chains. IT - Information Technology, 2022, .	0.9	0