Yiorgos Makris

List of Publications by Year
in descending order

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168	3,039	471061	315357
papers	citations	17 h-index	38 g-index

172	172	172	1245
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Phase Noise Reduction in LC VCOâ€™s Using an Array of Cross-Coupled Nanoscale MOSFETs and Intelligent Post-Fabrication Selection. IEEE Transactions on Microwave Theory and Techniques, 2022, 70, 3244-3256.	2.9	2
2	Genetic physical unclonable functions in human cells. Science Advances, 2022, 8, eabm4106.	4.7	4
3	Hunting Security Bugs in SoC Designs: Lessons Learned. IEEE Design and Test, 2021, 38, 22-29.	1.1	3
4	Improved Static Hand Gesture Classification on Deep Convolutional Neural Networks Using Novel Sterile Training Technique. IEEE Access, 2021, 9, 10893-10902.	2.6	28
5	On Improving Hotspot Detection Through Synthetic Pattern-Based Database Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2522-2527.	1.9	7
6	TPE: A Hardware-Based TLB Profiling Expert for Workload Reconstruction. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 292-305.	2.7	2
7	Proof-Carrying Hardware-Based Information Flow Tracking in Analog/Mixed-Signal Designs. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 415-427.	2.7	7
8	Bias Busters: Robustifying DL-Based Lithographic Hotspot Detectors Against Backdooring Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2077-2089.	1.9	2
9	Hardware-Induced Covert Channels in Wireless Networks: Risks and Remedies. , 2021, , 1-9.		0
10	Functional Locking through Omission: From HLS to Obfuscated Design. , 2021, , .		0
11	Automated Die Inking. IEEE Transactions on Device and Materials Reliability, 2020, 20, 295-307.	1.5	8
12	Range-Controlled Floating-Gate Transistors: A Unified Solution for Unlocking and Calibrating Analog ICs. , 2020, , .		12
13	An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs. , 2020, , .		2
14	CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric. , 2020, , .		0
15	Amplitude-Modulating Analog/RF Hardware Trojans in Wireless Networks: Risks and Remedies. IEEE Transactions on Information Forensics and Security, 2020, 15, 3497-3510.	4.5	10
16	ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric. , 2020, , .		0
17	A Hardware-Based Architecture-Neutral Framework for Real-Time IoT Workload Forensics. IEEE Transactions on Computers, 2020, 69, 1668-1680.	2.4	4
18	Hardware-Based Real-Time Workload Forensics. IEEE Design and Test, 2020, 37, 52-58.	1.1	2

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19	DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY. , 2020, , .		17
20	Analog Performance Locking through Neural Network-Based Biasing. , 2019, , .		20
21	Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming. , 2019, , .		18
22	Post-Production Calibration of Analog/RF ICs: Recent Developments and A Fully Integrated Solution. , 2019, , .		2
23	Hardware-based Real-time Workload Forensics via Frame-level TLB Profiling. , 2019, , .		2
24	Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA. , 2019, , .		18
25	CAPE: A cross-layer framework for accurate microprocessor power estimation. The Integration VLSI Journal, 2019, 68, 87-98.	1.3	0
26	Demonstrating and Mitigating the Risk of an FEC-Based Hardware Trojan in Wireless Networks. IEEE Transactions on Information Forensics and Security, 2019, 14, 2720-2734.	4.5	13
27	Subtle Anomaly Detection of Microscopic Probes using Deep learning based Image Completion. , 2019, , .		0
28	Revisiting Capacitor-Based Trojan Design. , 2019, , .		1
29	VIPER: A Versatile and Intuitive Pattern GenERator for Early Design Space Exploration. , 2019, , .		2
30	Design Space Exploration for Hotspot Detection. , 2019, , .		0
31	Machine Learning-Based Hotspot Detection: Fallacies, Pitfalls and Marching Orders. , 2019, , .		15
32	Automated Die Inking through On-line Machine Learning. , 2019, , .		2
33	Extending the Lifetime of Coarse-Grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage. , 2019, , .		0
34	Wafer-Level Adaptive Vmin Calibration Seed Forecasting. , 2019, , .		0
35	Trusted and Secure Design of Analog/RF ICs: Recent Developments. , 2019, , .		5
36	Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications. , 2019, , 119-173.		1

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37	Towards provably-secure performance locking. , 2018, , .		8
38	Hardware Dithering: A Run-Time Method for Trojan Neutralization in Wireless Cryptographic ICs. , 2018, , .		3
39	On the use of Bayesian Networks for Resource-Efficient Self-Calibration of Analog/RF ICs. , 2018, , .		5
40	Towards a Cross-Layer Framework for Accurate Power Modeling of Microprocessor Designs. , 2018, , .		1
41	Hardware-assisted rootkit detection via on-line statistical fingerprinting of process execution. , 2018, , .		13
42	Special session on machine learning: How will machine learning transform test?. , 2018, , .		0
43	Enhanced hotspot detection through synthetic pattern generation and design of experiments. , 2018, , .		17
44	Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2120-2133.	1.9	11
45	A field programmable transistor array featuring single-cycle partial/full dynamic reconfiguration. , 2017, , .		6
46	Data Secrecy Protection Through Information Flow Tracking in Proof-Carrying Hardware IPâ€”Part II: Framework Automation. IEEE Transactions on Information Forensics and Security, 2017, 12, 2430-2443.	4.5	11
47	Hardware-based on-line intrusion detection via system call routine fingerprinting. , 2017, , .		9
48	Information flow tracking in analog/mixed-signal designs through proof-carrying hardware IP. , 2017, , .		16
49	Knob non-idealities in learning-based post-production tuning of analog/RF ICs: Impact & remedies. , 2017, , .		1
50	Data Secrecy Protection Through Information Flow Tracking in Proof-Carrying Hardware IPâ€”Part I: Framework Fundamentals. IEEE Transactions on Information Forensics and Security, 2017, 12, 2416-2429.	4.5	18
51	Silicon Demonstration of Hardware Trojan Design and Detection in Wireless Cryptographic ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1506-1519.	2.1	81
52	Trusted Analog/Mixed- Signal/RF ICs: A Survey and a Perspective. IEEE Design and Test, 2017, 34, 63-76.	1.1	21
53	INFECT: INconspicuous FEC-based Trojan: A hardware attack on an 802.11a/g wireless network. , 2017, , .		11
54	Security and trust in the analog/mixed-signal/RF domain: A survey and a perspective. , 2017, , .		13

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55	Automated die inking: A pattern recognition-based approach. , 2017, , .		7
56	ACE: Adaptive channel estimation for detecting analog/RF trojans in WLAN transceivers. , 2017, , .		13
57	Wafer-level adaptive trim seed forecasting based on E-tests. , 2017, , .		3
58	What to Lock?. , 2017, , .		71
59	Hardware-based workload forensics: Process reconstruction via TLB monitoring. , 2016, , .		9
60	Hardware-based attacks to compromise the cryptographic security of an election system. , 2016, , .		8
61	Hardware-Based Workload Forensics and Malware Detection in Microprocessors. , 2016, , .		2
62	Harnessing fabrication process signature for predicting yield across designs. , 2016, , .		2
63	Harnessing process variations for optimizing wafer-level probe-test flow. , 2016, , .		6
64	A machine learning approach to fab-of-origin attestation. , 2016, , .		7
65	Wafer-level process variation-driven probe-test flow selection for test cost reduction in analog/RF ICs. , 2016, , .		9
66	Toward Silicon-Based Cognitive Neuromorphic ICsâ€"A Survey. IEEE Design and Test, 2016, 33, 91-102.	1.1	9
67	On-die learning-based self-calibration of analog/RF ICs. , 2016, , .		10
68	Hardware Trojan Detection in Analog/RF Integrated Circuits. , 2016, , 241-268.		5
69	Yield forecasting in fab-to-fab production migration based on Bayesian Model Fusion. , 2015, , .		6
70	Silicon Demonstration of Statistical Post-Production Tuning. , 2015, , .		3
71	Recycled IC Detection Based on Statistical Methods. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 947-960.	1.9	43
72	A comparative study of one-shot statistical calibration methods for analog / RF ICs. , 2015, , .		18

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73	Yield prognosis for fab-to-fab product migration. , 2015, , .		3
74	An Experimentation Platform for On-Chip Integration of Analog Neural Networks: A Pathway to Trusted and Robust Analog/RF ICs. IEEE Transactions on Neural Networks and Learning Systems, 2015, 26, 1721-1734.	7.2	14
75	Concurrent hardware Trojan detection in wireless cryptographic ICs. , 2015, , .		23
76	Multiple-Bit Upset Protection in Microprocessor Memory Arrays Using Vulnerability-Based Parity Optimization and Interleaving. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2447-2460.	2.1	13
77	Guest Editorial Special Section on Hardware Security and Trust. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 873-874.	1.9	3
78	Revisiting Vulnerability Analysis in Modern Microprocessors. IEEE Transactions on Computers, 2015, 64, 2664-2674.	2.4	9
79	VeriCoq: A Verilog-to-Coq converter for proof-carrying hardware automation. , 2015, , .		16
80	Toward automatic proof generation for information flow policies in third-party hardware IP. , 2015, , .		24
81	Workload characterization and prediction: A pathway to reliable multi-core systems. , 2015, , .		9
82	IC laser trimming speed-up through wafer-level spatial correlation modeling. , 2014, , .		5
83	Low-Cost Analog/RF IC Testing through Combined Intra- and Inter-Die Correlation Models. IEEE Design and Test, 2014, , 1-1.	1.1	6
84	Spatio-temporal wafer-level correlation modeling with progressive sampling: A pathway to HVM yield estimation. , 2014, , .		8
85	Hardware Trojan Detection through Golden Chip-Free Statistical Side-Channel Fingerprinting. , 2014, , .		26
86	An analog non-volatile neural network platform for prototyping RF BIST solutions. , 2014, , .		0
87	Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain. Proceedings of the IEEE, 2014, 102, 1207-1228.	16.4	384
88	On-chip intelligence: A pathway to self-testable, tunable, and trusted analog/RF ICs. , 2014, , .		2
89	Hardware Trojan detection through golden chip-free statistical side-channel fingerprinting. , 2014, , .		26
90	An analog non-volatile neural network platform for prototyping RF BIST solutions. , 2014, , .		0

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91	On the Impact of Performance Faults in Modern Microprocessors. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 351-366.	0.9	3
92	A post-deployment IC trust evaluation architecture. , 2013, , .		5
93	Cycle-accurate information assurance by proof-carrying based signal sensitivity tracing. , 2013, , .		40
94	AVF-driven Parity Optimization for MBU Protection of In-core Memory Arrays. , 2013, , .		4
95	Handling Discontinuous Effects in Modeling Spatial Correlation of Wafer-level Analog/RF Tests. , 2013, , .		16
96	Counterfeit electronics: A rising threat in the semiconductor manufacturing industry. , 2013, , .		24
97	Process monitoring through wafer-level spatial variation decomposition. , 2013, , .		15
98	On combining alternate test with spatial correlation modeling in analog/RF ICs. , 2013, , .		7
99	Hardware Trojans in wireless cryptographic ICs: Silicon demonstration & detection method evaluation. , 2013, , .		43
100	Investigating the limits of AVF analysis in the presence of multiple bit errors. , 2013, , .		5
101	Hardware Trojans in Wireless Cryptographic Integrated Circuits. IEEE Design and Test, 2013, , 1-1.	1.1	6
102	A proof-carrying based framework for trusted microprocessor IP. , 2013, , .		28
103	Spatial correlation modeling for probe test cost reduction in RF devices. , 2012, , .		24
104	Proof-Carrying Hardware Intellectual Property: A Pathway to Trusted Module Acquisition. IEEE Transactions on Information Forensics and Security, 2012, 7, 25-40.	4.5	143
105	Integrated optimization of semiconductor manufacturing: A machine learning approach. , 2012, , .		6
106	A dual-mode weight storage analog neural network platform for on-chip applications. , 2012, , .		5
107	Post-deployment trust evaluation in wireless cryptographic ICs. , 2012, , .		5
108	Proof carrying-based information flow tracking for data secrecy protection and hardware trust. , 2012, , .		52

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109	Applying the Model-View-Controller Paradigm to Adaptive Test. IEEE Design and Test of Computers, 2012, 29, 28-35.	1.4	8
110	Spatial estimation of wafer measurement parameters using Gaussian process models. , 2012, , .		20
111	Towards a fully stand-alone analog/RF BIST: A cost-effective implementation of a neural classifier. , 2012, , .		1
112	Exposing vulnerabilities of untrusted computing platforms. , 2012, , .		26
113	Parametric counterfeit IC detection via Support Vector Machines. , 2012, , .		59
114	Vulnerability-based Interleaving for Multi-Bit Upset (MBU) protection in modern microprocessors. , 2012, , .		5
115	Global Signal Vulnerability (GSV) Analysis for Selective State Element Hardening in Modern Microprocessors. IEEE Transactions on Computers, 2012, 61, 1361-1370.	2.4	2
116	Design for Hardware Trust. , 2012, , 365-384.		4
117	AVF Analysis Acceleration via Hierarchical Fault Pruning. , 2011, , .		13
118	On proving the efficiency of alternative RF tests. , 2011, , .		9
119	Is single-scheme Trojan prevention sufficient?. , 2011, , .		1
120	Exponent monitoring for low-cost concurrent error detection in FPU control logic. , 2011, , .		7
121	PSCML: Pseudo-Static Current Mode Logic. , 2011, , .		1
122	Enhancing security via provably trustworthy hardware intellectual property. , 2011, , .		25
123	Guest Editors' Introduction: Special Section on Chips and Architectures for Emerging Technologies and Applications. IEEE Transactions on Computers, 2011, 60, 450-451.	2.4	0
124	Improving Analog and RF Device Yield through Performance Calibration. IEEE Design and Test of Computers, 2011, 28, 64-75.	1.4	26
125	Workload-Cognizant Concurrent Error Detection in the Scheduler of a Modern Microprocessor. IEEE Transactions on Computers, 2011, 60, 1274-1287.	2.4	2
126	Instruction-Level Impact Analysis of Low-Level Faults in a Modern Microprocessor Controller. IEEE Transactions on Computers, 2011, 60, 1260-1273.	2.4	45

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127	PPM-accuracy Error Estimates for Low-Cost Analog Test: A Case Study. , 2011, , .		1
128	Correlating inline data with final test outcomes in analog/RF devices. , 2011, , .		14
129	An analog VLSI multilayer perceptron and its application towards built-in self-test in analog circuits. , 2010, , .		7
130	Hardware Trojans in Wireless Cryptographic ICs. IEEE Design and Test of Computers, 2010, 27, 26-35.	1.4	108
131	DFTT: Design for Trojan Test. , 2010, , .		14
132	RF Specification Test Compaction Using Learning Machines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 998-1002.	2.1	40
133	Workload-driven selective hardening of control state elements in modern microprocessors. , 2010, , .		19
134	Analog neural network design for RF built-in self-test. , 2010, , .		24
135	Post-production performance calibration in analog/RF devices. , 2010, , .		24
136	Experiences in Hardware Trojan design and implementation. , 2009, , .		165
137	Instruction-Level Impact Comparison of RT- vs. Gate-Level Faults in a Modern Microprocessor Controller. , 2009, , .		3
138	Enrichment of limited training sets in machine-learning-based analog/RF test. , 2009, , .		21
139	On Boosting the Accuracy of Non-RF to RF Correlation-Based Specification Test Compaction. Journal of Electronic Testing: Theory and Applications (JETTA), 2009, 25, 309-321.	0.9	13
140	Special Session 7C: TTTC 2009 Best Doctoral Thesis Contest. , 2009, , .		0
141	Impact analysis of performance faults in modern microprocessors. , 2009, , .		9
142	Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 869-882.	2.1	12
143	Enhancing Simulation Accuracy through Advanced Hazard Detection in Asynchronous Circuits. IEEE Transactions on Computers, 2009, 58, 394-408.	2.4	4
144	Soft Error Mitigation Through Selective Addition of Functionally Redundant Wires. IEEE Transactions on Reliability, 2008, 57, 23-31.	3.5	42

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145	Coping with Soft Errors in Asynchronous Burst-Mode Machines. , 2008, , .		7
146	Error Moderation in Low-Cost Machine-Learning-Based Analog/RF Testing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 339-351.	1.9	103
147	A Statistical Approach to Characterizing and Testing Functionalized Nanowires. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	0
148	Design and Evaluation of a Timestamp-Based Concurrent Error Detection Method (CED) in a Modern Microprocessor Controller. , 2008, , .		7
149	On the Correlation between Controller Faults and Instruction-Level Errors in Modern Microprocessors. , 2008, , .		19
150	On the Minimization of Potential Transient Errors and SER in Logic Circuits Using SPFD. , 2008, , .		4
151	Hardware Trojan detection using path delay fingerprint. , 2008, , .		183
152	Confidence Estimation in Non-RF to RF Correlation-Based Specification Test Compaction. , 2008, , .		17
153	Concurrent Error Detection Methods for Asynchronous Burst-Mode Machines. IEEE Transactions on Computers, 2007, 56, 785-798.	2.4	19
154	Non-RF to RF Test Correlation Using Learning Machines: A Case Study. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	54
155	On the identification of modular test requirements for low cost hierarchical test path construction. The Integration VLSI Journal, 2007, 40, 315-325.	1.3	1
156	Testing Delay Faults in Asynchronous Handshake Circuits. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	4
157	Seamless Integration of SER in Rewiring-Based Design Space Exploration. IEEE International Test Conference (TC), 2006, , .	0.0	23
158	An Adaptive Checker for the Fully Differential Analog Code. IEEE Journal of Solid-State Circuits, 2006, 41, 1421-1429.	3.5	23
159	Compaction-based concurrent error detection for digital circuits. Microelectronics Journal, 2005, 36, 856-862.	1.1	6
160	Generating decision regions in analog measurement spaces. , 2005, , .		1
161	Fault simulation and random test generation for speed-independent circuits. , 2004, , .		7
162	Enhancing Reliability of RTL Controller-Datapath Circuits via Invariant-Based Concurrent Test. IEEE Transactions on Reliability, 2004, 53, 269-278.	3.5	12

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163	An Analog Checker with Input-Relative Tolerance for Duplicate Signals. Journal of Electronic Testing: Theory and Applications (JETTA), 2004, 20, 479-488.	0.9	8
164	SPaRre: selective partial replication for concurrent fault-detection in FSMs. IEEE Transactions on Instrumentation and Measurement, 2003, 52, 1729-1737.	2.4	25
165	Fast Hierarchical Test Path Construction for Circuits with DFT-Free Controller-Datapath Interface. Journal of Electronic Testing: Theory and Applications (JETTA), 2002, 18, 29-42.	0.9	3
166	RTL Test Justification and Propagation Analysis for Modular Designs. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 105-120.	0.9	34
167	On compaction-based concurrent error detection. , 0, , .		0
168	Test generation for ultra-high-speed asynchronous pipelines. , 0, , .		12