Yiorgos Makris

List of Publications by Year
in descending order

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168 papers	3,039 citations	471509 17 h-index	315739 38 g-index
172 all docs	172 docs citations	172 times ranked	1245 citing authors

#	Article	IF	Citations
1	Counterfeit Integrated Circuits: A Rising Threat in the Global Semiconductor Supply Chain. Proceedings of the IEEE, 2014, 102, 1207-1228.	21.3	384
2	Hardware Trojan detection using path delay fingerprint. , 2008, , .		183
3	Experiences in Hardware Trojan design and implementation. , 2009, , .		165
4	Proof-Carrying Hardware Intellectual Property: A Pathway to Trusted Module Acquisition. IEEE Transactions on Information Forensics and Security, 2012, 7, 25-40.	6.9	143
5	Hardware Trojans in Wireless Cryptographic ICs. IEEE Design and Test of Computers, 2010, 27, 26-35.	1.0	108
6	Error Moderation in Low-Cost Machine-Learning-Based Analog/RF Testing. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 339-351.	2.7	103
7	Silicon Demonstration of Hardware Trojan Design and Detection in Wireless Cryptographic ICs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1506-1519.	3.1	81
8	What to Lock?. , 2017, , .		71
9	Parametric counterfeit IC detection via Support Vector Machines. , 2012, , .		59
10	Non-RF to RF Test Correlation Using Learning Machines: A Case Study. VLSI Test Symposium (VTS), Proceedings, IEEE, 2007, , .	1.0	54
11	Proof carrying-based information flow tracking for data secrecy protection and hardware trust. , 2012, , .		52
12	Instruction-Level Impact Analysis of Low-Level Faults in a Modern Microprocessor Controller. IEEE Transactions on Computers, 2011, 60, 1260-1273.	3.4	45
13	Hardware Trojans in wireless cryptographic ICs: Silicon demonstration & detection method evaluation. , 2013, , .		43
14	Recycled IC Detection Based on Statistical Methods. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 947-960.	2.7	43
15	Soft Error Mitigation Through Selective Addition of Functionally Redundant Wires. IEEE Transactions on Reliability, 2008, 57, 23-31.	4.6	42
16	RF Specification Test Compaction Using Learning Machines. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 998-1002.	3.1	40
17	Cycle-accurate information assurance by proof-carrying based signal sensitivity tracing. , 2013, , .		40
18	RTL Test Justification and Propagation Analysis for Modular Designs. Journal of Electronic Testing: Theory and Applications (JETTA), 1998, 13, 105-120.	1.2	34

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19	A proof-carrying based framework for trusted microprocessor IP. , 2013, , .		28
20	Improved Static Hand Gesture Classification on Deep Convolutional Neural Networks Using Novel Sterile Training Technique. IEEE Access, 2021, 9, 10893-10902.	4.2	28
21	Improving Analog and RF Device Yield through Performance Calibration. IEEE Design and Test of Computers, 2011, 28, 64-75.	1.0	26
22	Exposing vulnerabilities of untrusted computing platforms. , 2012, , .		26
23	Hardware Trojan Detection through Golden Chip-Free Statistical Side-Channel Fingerprinting. , 2014, , .		26
24	Hardware Trojan detection through golden chip-free statistical side-channel fingerprinting. , 2014, , .		26
25	SPaRre: selective partial replication for concurrent fault-detection in FSMs. IEEE Transactions on Instrumentation and Measurement, 2003, 52, 1729-1737.	4.7	25
26	Enhancing security via provably trustworthy hardware intellectual property. , 2011, , .		25
27	Analog neural network design for RF built-in self-test. , 2010, , .		24
28	Post-production performance calibration in analog/RF devices. , 2010, , .		24
29	Spatial correlation modeling for probe test cost reduction in RF devices. , 2012, , .		24
30	Counterfeit electronics: A rising threat in the semiconductor manufacturing industry. , 2013, , .		24
31	Toward automatic proof generation for information flow policies in third-party hardware IP. , 2015, , .		24
32	Seamless Integration of SER in Rewiring-Based Design Space Exploration. IEEE International Test Conference (TC), 2006, , .	0.0	23
33	An Adaptive Checker for the Fully Differential Analog Code. IEEE Journal of Solid-State Circuits, 2006, 41, 1421-1429.	5.4	23
34	Concurrent hardware Trojan detection in wireless cryptographic ICs. , 2015, , .		23
35	Enrichment of limited training sets in machine-learning-based analog/RF test. , 2009, , .		21
36	Trusted Analog/Mixed- Signal/RF ICs: A Survey and a Perspective. IEEE Design and Test, 2017, 34, 63-76.	1.2	21

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37	Spatial estimation of wafer measurement parameters using Gaussian process models. , 2012, , .		20
38	Analog Performance Locking through Neural Network-Based Biasing. , 2019, , .		20
39	Concurrent Error Detection Methods for Asynchronous Burst-Mode Machines. IEEE Transactions on Computers, 2007, 56, 785-798.	3.4	19
40	On the Correlation between Controller Faults and Instruction-Level Errors in Modern Microprocessors. , 2008, , .		19
41	Workload-driven selective hardening of control state elements in modern microprocessors. , 2010, , .		19
42	A comparative study of one-shot statistical calibration methods for analog / RF ICs. , 2015, , .		18
43	Data Secrecy Protection Through Information Flow Tracking in Proof-Carrying Hardware IPâ€"Part I: Framework Fundamentals. IEEE Transactions on Information Forensics and Security, 2017, 12, 2416-2429.	6.9	18
44	Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming. , 2019, , .		18
45	Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA. , 2019, , .		18
46	Confidence Estimation in Non-RF to RF Correlation-Based Specification Test Compaction. , 2008, , .		17
47	Enhanced hotspot detection through synthetic pattern generation and design of experiments. , 2018, , .		17
48	DECOY: DEflection-Driven HLS-Based Computation Partitioning for Obfuscating Intellectual PropertY. , 2020, , .		17
49	Handling Discontinuous Effects in Modeling Spatial Correlation of Wafer-level Analog/RF Tests. , 2013, , .		16
50	VeriCoq: A Verilog-to-Coq converter for proof-carrying hardware automation. , 2015, , .		16
51	Information flow tracking in analog/mixed-signal designs through proof-carrying hardware IP. , 2017, , .		16
52	Process monitoring through wafer-level spatial variation decomposition. , 2013, , .		15
53	Machine Learning-Based Hotspot Detection: Fallacies, Pitfalls and Marching Orders. , 2019, , .		15
54	DFTT: Design for Trojan Test. , 2010, , .		14

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55	Correlating inline data with final test outcomes in analog/RF devices. , 2011, , .		14
56	An Experimentation Platform for On-Chip Integration of Analog Neural Networks: A Pathway to Trusted and Robust Analog/RF ICs. IEEE Transactions on Neural Networks and Learning Systems, 2015, 26, 1721-1734.	11.3	14
57	On Boosting the Accuracy of Non-RF to RF Correlation-Based Specification Test Compaction. Journal of Electronic Testing: Theory and Applications (JETTA), 2009, 25, 309-321.	1.2	13
58	AVF Analysis Acceleration via Hierarchical Fault Pruning. , 2011, , .		13
59	Multiple-Bit Upset Protection in Microprocessor Memory Arrays Using Vulnerability-Based Parity Optimization and Interleaving. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2447-2460.	3.1	13
60	Security and trust in the analog/mixed-signal/RF domain: A survey and a perspective. , 2017, , .		13
61	ACE: Adaptive channel estimation for detecting analog/RF trojans in WLAN transceivers. , 2017, , .		13
62	Hardware-assisted rootkit detection via on-line statistical fingerprinting of process execution. , 2018, , .		13
63	Demonstrating and Mitigating the Risk of an FEC-Based Hardware Trojan in Wireless Networks. IEEE Transactions on Information Forensics and Security, 2019, 14, 2720-2734.	6.9	13
64	Enhancing Reliability of RTL Controller-Datapath Circuits via Invariant-Based Concurrent Test. IEEE Transactions on Reliability, 2004, 53, 269-278.	4.6	12
65	Test generation for ultra-high-speed asynchronous pipelines. , 0, , .		12
66	Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 869-882.	3.1	12
67	Range-Controlled Floating-Gate Transistors: A Unified Solution for Unlocking and Calibrating Analog ICs. , 2020, , .		12
68	Yield Forecasting Across Semiconductor Fabrication Plants and Design Generations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 2120-2133.	2.7	11
69	Data Secrecy Protection Through Information Flow Tracking in Proof-Carrying Hardware IPâ€"Part II: Framework Automation. IEEE Transactions on Information Forensics and Security, 2017, 12, 2430-2443.	6.9	11
70	INFECT: INconspicuous FEC-based Trojan: A hardware attack on an 802.11a/g wireless network. , 2017, , .		11
71	On-die learning-based self-calibration of analog/RF ICs. , 2016, , .		10
72	Amplitude-Modulating Analog/RF Hardware Trojans in Wireless Networks: Risks and Remedies. IEEE Transactions on Information Forensics and Security, 2020, 15, 3497-3510.	6.9	10

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73	Impact analysis of performance faults in modern microprocessors. , 2009, , .		9
74	On proving the efficiency of alternative RF tests. , 2011, , .		9
75	Revisiting Vulnerability Analysis in Modern Microprocessors. IEEE Transactions on Computers, 2015, 64, 2664-2674.	3.4	9
76	Workload characterization and prediction: A pathway to reliable multi-core systems. , 2015, , .		9
77	Hardware-based workload forensics: Process reconstruction via TLB monitoring. , 2016, , .		9
78	Wafer-level process variation-driven probe-test flow selection for test cost reduction in analog/RF ICs. , 2016, , .		9
79	Toward Silicon-Based Cognitive Neuromorphic ICsâ€"A Survey. IEEE Design and Test, 2016, 33, 91-102.	1.2	9
80	Hardware-based on-line intrusion detection via system call routine fingerprinting. , 2017, , .		9
81	An Analog Checker with Input-Relative Tolerance for Duplicate Signals. Journal of Electronic Testing: Theory and Applications (JETTA), 2004, 20, 479-488.	1.2	8
82	Applying the Model-View-Controller Paradigm to Adaptive Test. IEEE Design and Test of Computers, 2012, 29, 28-35.	1.0	8
83	Spatio-temporal wafer-level correlation modeling with progressive sampling: A pathway to HVM yield estimation. , 2014, , .		8
84	Hardware-based attacks to compromise the cryptographic security of an election system. , 2016, , .		8
85	Towards provably-secure performance locking. , 2018, , .		8
86	Automated Die Inking. IEEE Transactions on Device and Materials Reliability, 2020, 20, 295-307.	2.0	8
87	Fault simulation and random test generation for speed-independent circuits. , 2004, , .		7
88	Coping with Soft Errors in Asynchronous Burst-Mode Machines. , 2008, , .		7
89	Design and Evaluation of a Timestamp-Based Concurrent Error Detection Method (CED) in a Modern Microprocessor Controller. , 2008, , .		7
90	An analog VLSI multilayer perceptron and its application towards built-in self-test in analog circuits. , 2010, , .		7

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91	Exponent monitoring for low-cost concurrent error detection in FPU control logic. , 2011, , .		7
92	On combining alternate test with spatial correlation modeling in analog/RF ICs. , 2013, , .		7
93	A machine learning approach to fab-of-origin attestation. , 2016, , .		7
94	Automated die inking: A pattern recognition-based approach. , 2017, , .		7
95	On Improving Hotspot Detection Through Synthetic Pattern-Based Database Enhancement. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2522-2527.	2.7	7
96	Proof-Carrying Hardware-Based Information Flow Tracking in Analog/Mixed-Signal Designs. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 415-427.	3.6	7
97	Compaction-based concurrent error detection for digital circuits. Microelectronics Journal, 2005, 36, 856-862.	2.0	6
98	Integrated optimization of semiconductor manufacturing: A machine learning approach. , 2012, , .		6
99	Hardware Trojans in Wireless Cryptographic Integrated Circuits. IEEE Design and Test, 2013, , 1-1.	1.2	6
100	Low-Cost Analog/RF IC Testing through Combined Intra- and Inter-Die Correlation Models. IEEE Design and Test, 2014, , 1-1.	1.2	6
101	Yield forecasting in fab-to-fab production migration based on Bayesian Model Fusion. , 2015, , .		6
102	Harnessing process variations for optimizing wafer-level probe-test flow. , 2016, , .		6
103	A field programmable transistor array featuring single-cycle partial/full dynamic reconfiguration. , 2017, , .		6
104	A dual-mode weight storage analog neural network platform for on-chip applications. , 2012, , .		5
105	Post-deployment trust evaluation in wireless cryptographic ICs. , 2012, , .		5
106	Vulnerability-based Interleaving for Multi-Bit Upset (MBU) protection in modern microprocessors. , 2012, , .		5
107	A post-deployment IC trust evaluation architecture. , 2013, , .		5
108	Investigating the limits of AVF analysis in the presence of multiple bit errors. , 2013, , .		5

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109	IC laser trimming speed-up through wafer-level spatial correlation modeling. , 2014, , .		5
110	On the use of Bayesian Networks for Resource-Efficient Self-Calibration of Analog/RF ICs. , 2018, , .		5
111	Trusted and Secure Design of Analog/RF ICs: Recent Developments. , 2019, , .		5
112	Hardware Trojan Detection in Analog/RF Integrated Circuits. , 2016, , 241-268.		5
113	Testing Delay Faults in Asynchronous Handshake Circuits. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	4
114	On the Minimization of Potential Transient Errors and SER in Logic Circuits Using SPFD. , 2008, , .		4
115	Enhancing Simulation Accuracy through Advanced Hazard Detection in Asynchronous Circuits. IEEE Transactions on Computers, 2009, 58, 394-408.	3.4	4
116	AVF-driven Parity Optimization for MBU Protection of In-core Memory Arrays. , 2013, , .		4
117	A Hardware-Based Architecture-Neutral Framework for Real-Time IoT Workload Forensics. IEEE Transactions on Computers, 2020, 69, 1668-1680.	3.4	4
118	Design for Hardware Trust. , 2012, , 365-384.		4
119	Genetic physical unclonable functions in human cells. Science Advances, 2022, 8, eabm4106.	10.3	4
120	Fast Hierarchical Test Path Construction for Circuits with DFT-Free Controller-Datapath Interface. Journal of Electronic Testing: Theory and Applications (JETTA), 2002, 18, 29-42.	1.2	3
121	Instruction-Level Impact Comparison of RT- vs. Gate-Level Faults in a Modern Microprocessor Controller. , 2009, , .		3
122	On the Impact of Performance Faults in Modern Microprocessors. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 351-366.	1.2	3
123	Silicon Demonstration of Statistical Post-Production Tuning. , 2015, , .		3
124	Yield prognosis for fab-to-fab product migration. , 2015, , .		3
125	Guest Editorial Special Section on Hardware Security and Trust. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 873-874.	2.7	3
126	Wafer-level adaptive trim seed forecasting based on E-tests. , 2017, , .		3

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127	Hardware Dithering: A Run-Time Method for Trojan Neutralization in Wireless Cryptographic ICs. , 2018, , .		3
128	Hunting Security Bugs in SoC Designs: Lessons Learned. IEEE Design and Test, 2021, 38, 22-29.	1.2	3
129	Workload-Cognizant Concurrent Error Detection in the Scheduler of a Modern Microprocessor. IEEE Transactions on Computers, 2011, 60, 1274-1287.	3.4	2
130	Global Signal Vulnerability (GSV) Analysis for Selective State Element Hardening in Modern Microprocessors. IEEE Transactions on Computers, 2012, 61, 1361-1370.	3.4	2
131	On-chip intelligence: A pathway to self-testable, tunable, and trusted analog/RF ICs. , 2014, , .		2
132	Hardware-Based Workload Forensics and Malware Detection in Microprocessors. , 2016, , .		2
133	Harnessing fabrication process signature for predicting yield across designs. , 2016, , .		2
134	Post-Production Calibration of Analog/RF ICs: Recent Developments and A Fully Integrated Solution. , 2019, , .		2
135	Hardware-based Real-time Workload Forensics via Frame-level TLB Profiling. , 2019, , .		2
136	VIPER: A Versatile and Intuitive Pattern GenERator for Early Design Space Exploration. , 2019, , .		2
137	Automated Die Inking through On-line Machine Learning. , 2019, , .		2
138	An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs. , 2020, , .		2
139	Hardware-Based Real-Time Workload Forensics. IEEE Design and Test, 2020, 37, 52-58.	1.2	2
140	TPE: A Hardware-Based TLB Profiling Expert for Workload Reconstruction. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 292-305.	3.6	2
141	Bias Busters: Robustifying DL-Based Lithographic Hotspot Detectors Against Backdooring Attacks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 2077-2089.	2.7	2
142	Phase Noise Reduction in LC VCOâ€™s Using an Array of Cross-Coupled Nanoscale MOSFETs and Intelligent Post-Fabrication Selection. IEEE Transactions on Microwave Theory and Techniques, 2022, 70, 3244-3256.	4.6	2
143	Generating decision regions in analog measurement spaces. , 2005, , .		1
144	On the identification of modular test requirements for low cost hierarchical test path construction. The Integration VLSI Journal, 2007, 40, 315-325.	2.1	1

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145	Is single-scheme Trojan prevention sufficient?. , 2011, , .		1
146	PSCML: Pseudo-Static Current Mode Logic. , 2011, , .		1
147	PPM-accuracy Error Estimates for Low-Cost Analog Test: A Case Study. , 2011, , .		1
148	Towards a fully stand-alone analog/RF BIST: A cost-effective implementation of a neural classifier. , 2012, , .		1
149	Knob non-idealities in learning-based post-production tuning of analog/RF ICs: Impact & remedies. , 2017, , .		1
150	Towards a Cross-Layer Framework for Accurate Power Modeling of Microprocessor Designs. , 2018, , .		1
151	Revisiting Capacitor-Based Trojan Design. , 2019, , .		1
152	Gaussian Process-Based Wafer-Level Correlation Modeling and Its Applications. , 2019, , 119-173.		1
153	On compaction-based concurrent error detection. , 0, , .		0
154	A Statistical Approach to Characterizing and Testing Functionalized Nanowires. VLSI Test Symposium (VTS), Proceedings, IEEE, 2008, , .	1.0	0
155	Special Session 7C: TTTC 2009 Best Doctoral Thesis Contest. , 2009, , .		0
156	Guest Editors' Introduction: Special Section on Chips and Architectures for Emerging Technologies and Applications. IEEE Transactions on Computers, 2011, 60, 450-451.	3.4	0
157	An analog non-volatile neural network platform for prototyping RF BIST solutions. , 2014, , .		0
158	Special session on machine learning: How will machine learning transform test?. , 2018, , .		0
159	CAPE: A cross-layer framework for accurate microprocessor power estimation. The Integration VLSI Journal, 2019, 68, 87-98.	2.1	0
160	Subtle Anomaly Detection of Microscopic Probes using Deep learning based Image Completion. , 2019, , .		0
161	Design Space Exploration for Hotspot Detection. , 2019, , .		0
162	Extending the Lifetime of Coarse-Grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage. , 2019, , .		0

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163	Wafer-Level Adaptive Vmin Calibration Seed Forecasting. , 2019, , .		0
164	CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric. , 2020, , .		0
165	ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric. , 2020, , .		0
166	Hardware-Induced Covert Channels in Wireless Networks: Risks and Remedies. , 2021, , 1-9.		0
167	An analog non-volatile neural network platform for prototyping RF BIST solutions. , 2014, , .		0
168	Functional Locking through Omission: From HLS to Obfuscated Design. , 2021, , .		0