Igor Aleksejev

List of Publications by Year in descending order

Source: https://exaly.com/author-pdf/445557/publications.pdf

Version: 2024-02-01

3311381 2550090 17 61 3 1 citations g-index h-index papers 17 17 17 34 docs citations times ranked citing authors all docs

#	Article	IF	CITATIONS
1	FPGA-based synthetic instrumentation for board test. , 2012, , .		17
2	Fast extended test access via JTAG and FPGAs. , 2009, , .		13
3	Virtual reconfigurable scan-chains on FPGAs for optimized board test. , 2015, , .		5
4	Turning JTAG inside out for fast extended test access. , 2009, , .		4
5	Optimization of the Store-and-Generate Based Built-in Self-Test. International Biennial Baltic Electronics Conference, 2006, , .	0.0	3
6	Embedded synthetic instruments for Board-Level testing. , 2012, , .		3
7	Run-time reconfigurable instruments for advanced board-level testing. , 2016, , .		3
8	On coverage of timing related faults at board level. , 2016, , .		3
9	Teaching digital test with BIST analyzer. , 2008, , .		2
10	Reseeding using compaction of pre-generated LFSR sub-sequences. , 2008, , .		2
11	Application of Sequential Test Set Compaction to LFSR Reseeding. , 2008, , .		2
12	Optimization of Boundary Scan Tests Using FPGA-Based Efficient Scan Architectures. Journal of Electronic Testing: Theory and Applications (JETTA), 2016, 32, 245-255.	1.2	1
13	Run-time reconfigurable instruments for advanced board-level testing. IEEE Instrumentation and Measurement Magazine, 2017, 20, 23-30.	1.6	1
14	Embedded instrumentation toolbox for screening marginal defects and outliers for production. , 2017, , .		1
15	Ways for board and system test to benefit from FPGA embedded instrumentation. , $2019, \ldots$		1
16	Complex delay fault reasoning with sequential 7-valued algebra., 2015,,.		0
17	Sequential Test Set Compaction in LFSR Reseeding. Advances in Computer and Electrical Engineering Book Series, 0, , 476-493.	0.3	0