

# Chang-Chun Lee

## List of Publications by Year in descending order

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131  
papers

798  
citations

623734

14  
h-index

642732

23  
g-index

131  
all docs

131  
docs citations

131  
times ranked

573  
citing authors

#	ARTICLE	IF	CITATIONS
1	Investigation of solder crack behavior and fatigue life of the power module on different thermal cycling period. <i>Microelectronic Engineering</i> , 2013, 107, 125-129.	2.4	92
2	Light degradation test and design of thermal performance for high-power light-emitting diodes. <i>Microelectronics Reliability</i> , 2012, 52, 794-803.	1.7	36
3	Development of robust flexible OLED encapsulations using simulated estimations and experimental validations. <i>Journal Physics D: Applied Physics</i> , 2012, 45, 275102.	2.8	34
4	Open-loop altitude-azimuth concentrated solar tracking system for solar-thermal applications. <i>Solar Energy</i> , 2017, 147, 52-60.	6.1	30
5	Design and analysis of gasket sealing of cylinder head under engine operation conditions. <i>Finite Elements in Analysis and Design</i> , 2005, 41, 1160-1174.	3.2	28
6	Enhancing the Reliability of Wafer Level Packaging by Using Solder Joints Layout Design. <i>IEEE Transactions on Components and Packaging Technologies</i> , 2006, 29, 877-885.	1.3	27
7	Synthesis of mechanically robust epoxy cross-linked silica aerogel membranes for CO <sub>2</sub> capture. <i>Journal of the Taiwan Institute of Chemical Engineers</i> , 2018, 87, 117-122.	5.3	27
8	Modeling and validation of mechanical stress in indium tin oxide layer integrated in highly flexible stacked thin films. <i>Thin Solid Films</i> , 2013, 544, 443-447.	1.8	21
9	Packaging effect investigation of CMOS compatible pressure sensor using flip chip and flex circuit board technologies. <i>Sensors and Actuators A: Physical</i> , 2006, 126, 48-55.	4.1	19
10	Interfacial Fracture Investigation of Low-k Packaging Using J-Integral Methodology. <i>IEEE Transactions on Advanced Packaging</i> , 2008, 31, 91-99.	1.6	19
11	Reliability estimation and failure mode prediction for 3D chip stacking package with the application of wafer-level underfill. <i>Microelectronic Engineering</i> , 2013, 107, 107-113.	2.4	18
12	Solder joints layout design and reliability enhancement of wafer level packaging. , 0, , .		17
13	Nanonetwork Thermosets from Templated Polymerization for Enhanced Energy Dissipation. <i>Nano Letters</i> , 2021, 21, 3355-3363.	9.1	17
14	Interfacial Fracture Analysis of CMOS Cu/Low- $k$ BEOL Interconnect in Advanced Packaging Structures. <i>IEEE Transactions on Advanced Packaging</i> , 2009, 32, 53-61.	1.6	15
15	Development of Cu/Ni/SnAg Microbump Bonding Processes for Thin Chip-on-Chip Packages Via Wafer-Level Underfill Film. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2012, 2, 1412-1419.	2.5	15
16	Comparison of Mechanical Modeling to Warpage Estimation of RDL-First Fan-Out Panel-Level Packaging. <i>IEEE Transactions on Components, Packaging and Manufacturing Technology</i> , 2022, 12, 1100-1108.	2.5	15
17	Investigation of pre-bending substrate design in packaging assembly of an IGBT power module. <i>Microelectronic Engineering</i> , 2014, 120, 106-113.	2.4	14
18	Development of Equivalent Material Properties of Microbump for Simulating Chip Stacking Packaging. <i>Materials</i> , 2015, 8, 5121-5137.	2.9	14

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19	Experimental and Simulated Investigations of Thin Polymer Substrates with an Indium Tin Oxide Coating under Fatigue Bending Loadings. <i>Materials</i> , 2016, 9, 720.	2.9	14
20	3-D Structure Design and Reliability Analysis of Wafer Level Package With Stress Buffer Mechanism. <i>IEEE Transactions on Components and Packaging Technologies</i> , 2007, 30, 110-118.	1.3	13
21	Overview of interfacial fracture energy predictions for stacked thin films using a four-point bending framework. <i>Surface and Coatings Technology</i> , 2013, 237, 333-340.	4.8	13
22	Electrical characteristics and reliability performance of IGBT power device packaging by chip embedding technology. <i>Microelectronics Reliability</i> , 2015, 55, 2582-2588.	1.7	13
23	Sensitivity Design of DL-WLCSP Using DOE With Factorial Analysis Technology. <i>IEEE Transactions on Advanced Packaging</i> , 2007, 30, 44-55.	1.6	12
24	Reliability enhancements of chip-on-chip package with layout designs of microbumps. <i>Microelectronic Engineering</i> , 2014, 120, 138-145.	2.4	12
25	Solder joints layout design and reliability enhancements of wafer level packaging using response surface methodology. <i>Microelectronics Reliability</i> , 2007, 47, 196-204.	1.7	11
26	Cracking energy estimation of ultra low-k package using novel prediction approach combined with global-local modeling technique. <i>Microelectronic Engineering</i> , 2008, 85, 2079-2084.	2.4	11
27	Prediction of interfacial adhesion strength of nanoscale Al/TiN films passed through patterned BEOL interconnects. <i>Materials Science in Semiconductor Processing</i> , 2015, 39, 1-5.	4.0	10
28	Reliability-Based Design Guidance of Three-Dimensional Integrated Circuits Packaging Using Thermal Compression Bonding and Dummy Cu/Ni/SnAg Microbumps. <i>Journal of Electronic Packaging, Transactions of the ASME</i> , 2014, 136, .	1.8	9
29	3D structure design and reliability analysis of wafer level package with bubble-like stress buffer layer. , 0, , .		8
30	Adhesion investigation of low-k films system using 4-point bending test. <i>Thin Solid Films</i> , 2009, 517, 4875-4878.	1.8	8
31	Effect of Wafer Level Underfill on the Microbump Reliability of Ultrathin-Chip Stacking Type 3D-IC Assembly during Thermal Cycling Tests. <i>Materials</i> , 2017, 10, 1220.	2.9	8
32	Induced thermo-mechanical reliability of copper-filled TSV interposer by transient selective annealing technology. <i>Microelectronics Reliability</i> , 2015, 55, 2213-2219.	1.7	7
33	Flexural Capability of Patterned Transparent Conductive Substrate by Performing Electrical Measurements and Stress Simulations. <i>Materials</i> , 2016, 9, 850.	2.9	7
34	Dependent Analyses of Multilayered Material/Geometrical Characteristics on the Mechanical Reliability of Flexible Display Devices. <i>IEEE Transactions on Device and Materials Reliability</i> , 2018, 18, 639-642.	2.0	7
35	Stability of J-integral calculation in the crack growth of copper/low-K stacked structures. , 0, , .		6
36	Electromigration Characteristic of SnAg <sub>3.0</sub> Cu <sub>0.5</sub> Flip Chip Interconnection. <i>IEEE Transactions on Advanced Packaging</i> , 2010, 33, 189-195.	1.6	6

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37	Investigation of Optical and Flexible Characteristics for Organic-Based Cholesteric Liquid Crystal Display by Utilizing Bending and Torsion Loadings. Journal of Display Technology, 2015, 11, 682-688.	1.2	6
38	Demonstration of an Equivalent Material Approach for the Strain-Induced Reliability Estimation of Stacked-Chip Packaging. IEEE Transactions on Device and Materials Reliability, 2020, 20, 475-482.	2.0	6
39	Investigation of interconnect design on interfacial cracking energy of Al/TiN barriers under a flexural load. Thin Solid Films, 2013, 544, 530-536.	1.8	5
40	Evaluation of Die Strength by Using Finite Element Method With Experiment Validation. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2014, 4, 1152-1158.	2.5	5
41	Mechanical property effects of Si $\lambda^{\sim}$ xGe channel and stressed contact etching stop layer on nano-scaled n-type metal-oxide-semiconductor field effect transistors. Thin Solid Films, 2014, 557, 316-322.	1.8	5
42	Assembly technology development and failure analysis for three-dimensional integrated circuit integration with ultra-thin chip stacking. Microelectronic Engineering, 2016, 156, 24-29.	2.4	5
43	Mixed mode interfacial crack energy estimation of glass interposer and SiNx coatings by using fracture mechanics based computer methods and experimental validations. Theoretical and Applied Fracture Mechanics, 2018, 96, 790-794.	4.7	5
44	Comprehensive Investigation on Warpage Management of FOPLP with Multi Embedded Ring Designs. , 2019, , .		5
45	Adhesion enhancement of conductive graphene/PI substrates through a vacuum plasma system. Surface and Coatings Technology, 2020, 388, 125601.	4.8	5
46	A Resultant Stress Effect of Contact Etching Stop Layer and Geometrical Designs of Poly Gate on Nanoscaled nMOSFETs with a Si<math>\lambda^{\sim}</math>x<math>\lambda^{\sim}</math>/SUB>Ge<math>\lambda^{\sim}</math>x<math>\lambda^{\sim}</math>/SUB> Channel. Journal of Nanoscience and Nanotechnology, 2015, 15, 2173-2178.	0.9	4
47	Flatness enhancement of the embedded interposer of 3D-ICs by using ring-type framework designs. Microelectronic Engineering, 2016, 156, 30-36.	2.4	4
48	Interfacial fracture investigation of patterned active matrix OLED driven by amorphous-Si TFTs under film-type packaging technology. Applied Surface Science, 2020, 510, 145428.	6.1	4
49	Reliability evaluation of ultra thin 3D-IC package under the coupling load effects of the manufacturing process and temperature cycling test. Microelectronic Engineering, 2021, 244-246, 111572.	2.4	4
50	Warpage Estimation of Heterogeneous Panel-Level Fan-Out Package with Fine Line RDL and Extreme Thin Laminated Substrate Considering Molding Characteristics. , 2021, , .		4
51	Assembly Reliability and Molding Material Comparison of Miniature Integrated High Power Module With Insulated Metal Substrate. Journal of Electronic Packaging, Transactions of the ASME, 2022, 144, .	1.8	4
52	Stress-Induced Failure Predictions of Flexible Electronics with Nano-Scaled Thin-Films. Science of Advanced Materials, 2017, 9, 6-10.	0.7	4
53	Design of double layer WLCSP using DOE with factorial analysis technology. , 0, , .		3
54	A TCAD simulation study of impact of strain engineering on nanoscale strained Si NMOSFETs with a silicon-carbon alloy stressor. Thin Solid Films, 2009, 518, 1595-1598.	1.8	3

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55	Strain engineering of nanoscale Si MOS devices. <i>Thin Solid Films</i> , 2010, 518, S241-S245.	1.8	3
56	Strain Engineering of Nanoscale Si $\langle i \rangle$ -Type Metal-Oxide-Semiconductor Field-Effect Transistor Devices with SiGe Alloy Integrated with Contact-Etch-Stop Layer Stressors. <i>Journal of Nanoscience and Nanotechnology</i> , 2012, 12, 5402-5406.	0.9	3
57	A New Stress Migration Failure Mode in Highly Scaled Cu/Low- $k$ Interconnects. <i>IEEE Transactions on Device and Materials Reliability</i> , 2012, 12, 529-531.	2.0	3
58	Performance Investigation of Nanoscale Strained Ge pMOSFETs with a GeSn Alloy Stressor. <i>Journal of Nanoscience and Nanotechnology</i> , 2015, 15, 9158-9162.	0.9	3
59	Predictions and measurements of interfacial adhesion among encapsulated thin films of flexible devices. <i>Thin Solid Films</i> , 2015, 584, 154-160.	1.8	3
60	Development and demonstration of equivalent material characteristics for microbump arrays utilized in failure estimation of chip-on-chip packaging. , 2016, , .		3
61	Adhesion investigation of stacked coatings in organic light-emitting diode display architecture. <i>Surface and Coatings Technology</i> , 2016, 303, 226-231.	4.8	3
62	Layout Study of Strained Ge-Based pMOSFETs Integrated With S/D GeSn Alloy and CESL by Using Process-Oriented Stress Simulations. <i>IEEE Transactions on Electron Devices</i> , 2018, 65, 4975-4981.	3.0	3
63	Simulated and experimental demonstrations of interfacial adhesive strength for released layer utilized in flexible electronics. <i>Thin Solid Films</i> , 2020, 706, 138022.	1.8	3
64	Packaging reliability estimation of high-power device modules by utilizing silver sintering technology. <i>Microelectronics Reliability</i> , 2020, 114, 113890.	1.7	3
65	Analytical Model Developed for Precise Stress Estimation of Device Channel Within Advanced Planar MOSFET Architectures. <i>IEEE Transactions on Electron Devices</i> , 2020, 67, 1498-1505.	3.0	3
66	Performance characteristics of strained Ge p-FinFETs under the integration of lattice and self-heating stress enabled by process-oriented finite element simulation. <i>Applied Physics Express</i> , 2021, 14, 035504.	2.4	3
67	Micro Solder Joint Reliability and Warpage Investigations of Extremely Thin Double-Layered Stacked-Chip Packaging. <i>Journal of Electronic Packaging, Transactions of the ASME</i> , 2022, 144, .	1.8	3
68	Estimated approach development and experimental validation of residual stress-induced warpage under the SiN <sub>x</sub> PECVD coating process. <i>Surface and Coatings Technology</i> , 2022, 434, 128225.	4.8	3
69	Impact of channel width and dummy length on performance enhancement in p-type metal oxide semiconductor field effect transistor with a silicon-germanium alloy stressor. <i>Journal of Vacuum Science &amp; Technology B</i> , 2009, 27, 1256.	1.3	2
70	Fracture prediction of dissimilar thin film materials in Cu/low- $k$ packaging. <i>Journal of Materials Science: Materials in Electronics</i> , 2010, 21, 787-795.	2.2	2
71	Assembly reliability improvement of 3D-ICs packaging using pre-stuffed molding material. <i>Vacuum</i> , 2015, 118, 152-160.	3.5	2
72	Ge $\lambda$ Si $\lambda$ on Ge-based n-type metal $\lambda$ oxide semiconductor field-effect transistors by device simulation combined with high-order stress $\lambda$ piezoresistive relationships. <i>Thin Solid Films</i> , 2016, 602, 78-83.	1.8	2

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73	Layout designs of surface barrier coatings for boosting the capability of oxygen/vapor obstruction utilized in flexible electronics. Applied Surface Science, 2018, 436, 183-188.	6.1	2
74	Intrinsic Stress Effect of Fabricated Processes on the Warpage and Microbump Reliability of Thin-Type 3D-ICs Packaging. , 2018, , .		2
75	Simulation and Experimental Validations of EM/TM/SM Physical Reliability for Interconnects Utilized in Stretchable and Foldable Electronics. , 2019, , .		2
76	Drop Impact Analysis of AMOLED Display with Buffer Designs by Using Dynamic Finite Element Simulation. , 2019, , .		2
77	A Novel Warpage Reinforcement Architecture with RDL Interposer for Heterogeneous Integrated Packages. , 2020, , .		2
78	Stress Impact of the Annealing Procedure of Cu-Filled TSV Packaging on the Performance of Nano-Scaled MOSFETs Evaluated by an Analytical Solution and FEA-Based Submodeling Technique. Materials, 2021, 14, 5226.	2.9	2
79	Surface Properties of Nano-Film Type Patterning Electrode on Flexible Substrate for Bending Test. Science of Advanced Materials, 2017, 9, 17-21.	0.7	2
80	A hybrid bonding interconnection with a novel low-temperature bonding polymer system. , 2022, , .		2
81	Simulation of a nanoscale strained Si NMOSFET with a siliconâ€“carbon alloy stressor. Thin Solid Films, 2010, 518, S72-S75.	1.8	1
82	Mechanical reliability enhancement of flexible packaging with OLED display under bending loading conditions. , 2011, , .		1
83	Impact of Strain Engineering on Nanoscale Strained InGaAs MOSFET Devices. Journal of Nanoscience and Nanotechnology, 2011, 11, 5623-5627.	0.9	1
84	Technology computer-aided design simulation study for a strained InGaAs channel n-type metal-oxide-semiconductor field-effect transistor with a high-k dielectric oxide layer and a metal gate electrode. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2011, 29, 032203.	1.2	1
85	Stress Impact of a Tensile Contact Etch Stop Layer on Nanoscale Strained NMOSFETs Embedded with a Siliconâ€“Carbon Alloy Stressor. Journal of Nanoscience and Nanotechnology, 2012, 12, 5342-5346.	0.9	1
86	Evaluation of Cu/Ni/SnAg microbump bonding processes for thin-chip-on-chip package using a wafer-level underfill film. , 2012, , .		1
87	Patterned film effects on the adhesion of Al/TiN barrier using fracture-energy based finite element analysis. Surface and Coatings Technology, 2013, 215, 400-406.	4.8	1
88	Reliability enhancement of ultra-thin chip assembly module in 3D-ICs integrations by the assistance of molding compounds. , 2014, , .		1
89	Investigation of consequent process-induced stress for N-type metal oxide semiconductor field effect transistor with a sunken shallow trench isolation pattern. Thin Solid Films, 2014, 557, 323-328.	1.8	1
90	Effects of extended poly gate on the performance of strained P-type metal-oxide-semiconductor field-effect transistors with a narrow channel width. Thin Solid Films, 2014, 557, 311-315.	1.8	1

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91	Influence of Glass Transition Temperature of Underfill on the Stress Behavior and Reliability of Microjoints Within a Chip Stacking Architecture. Journal of Electronic Packaging, Transactions of the ASME, 2015, 137, .	1.8	1
92	The effect of CESL and dummy poly gate for n-type MOSFETs with short Si 0.75 Ge 0.25 channel. Vacuum, 2017, 140, 66-70.	3.5	1
93	Material lattice orientation effect of local Si 1-x Ge x stressors on the width dependence of high-k metal gate PMOSFETs. Current Applied Physics, 2018, 18, S2-S7.	2.4	1
94	The development of estimated methodology for interfacial adhesion of semiconductor coatings having an enormous mismatch extent. Applied Surface Science, 2018, 440, 202-208.	6.1	1
95	Development of Real-Time Measurement Platform for Stretchable and Rollable Functions of Flexible Electronics under Multiple Dynamic Loads. Micromachines, 2020, 11, 106.	2.9	1
96	Improvements of Stress Migration in Nano-Scaled Copper Interconnects. Science of Advanced Materials, 2017, 9, 11-16.	0.7	1
97	Comprehensive Stress Effect of Thin Coatings and Silicon-Carbon Lattice Mismatch on Nano-Scaled Transistors with Protruding Poly Gate. Journal of Nanoscience and Nanotechnology, 2020, 20, 760-768.	0.9	1
98	Process-induced warpage and stress estimation of through glass via embedded interposer carrier with ring-type framework. Microelectronics Reliability, 2022, 129, 114476.	1.7	1
99	Corrections to "Enhancing the reliability of wafer level packaging by using solder joints layout design". IEEE Transactions on Components and Packaging Technologies, 2007, 30, 190-190.	1.3	0
100	Carrier backscattering characteristics of nanoscale strained complementary metal-oxide-semiconductor devices featuring the optimal stress engineering. Journal of Vacuum Science & Technology B, 2009, 27, 1261.	1.3	0
101	Impact of strain engineering on InGaAs NMOSFET with an InGaAs alloy stressor. Thin Solid Films, 2010, 519, 1738-1742.	1.8	0
102	Effective moduli prediction for silicon interposer with high-density Cu-filled through-silicon via. , 2011, , .		0
103	Assembly analysis of Cu/Ni/SnAg microbump for stacking thin chips in a fine pitch package using a wafer-level underfill. , 2012, , .		0
104	Packaging designs and flexural stress estimation for thin-film types of OLED devices. , 2012, , .		0
105	Effect of layout arrangements on strained n-type metal-oxide-semiconductor field-effect transistors with silicon-carbon stressor. Thin Solid Films, 2012, 520, 6282-6286.	1.8	0
106	Novel assembly framework of bi-layered molding materials for 3D-ICs packaging. , 2013, , .		0
107	Physically based modeling for stress assessment in MOS devices. , 2014, , .		0
108	Design and optimization of a generalized wide-bandwidth white light system for Light-Eye Technology (LeyeT). , 2014, , .		0

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109	Simulation-based sensitivity estimation of the geometric effect of poly gates on nanoscale n-type metal-oxide-semiconductor field-effect transistors with silicon-carbon alloy. Thin Solid Films, 2014, 570, 336-342.	1.8	0
110	Effects of array type of dummy active diffused region and gate geometries on narrow NMOSFETs with SiC S/D stressors. , 2014, , .		0
111	Structural Optimizations of Silicon Based NMOSFETs with a Sunken STI Pattern by Using a Robust Stress Simulation Methodology. Journal of Nanoscience and Nanotechnology, 2015, 15, 2179-2184.	0.9	0
112	Fabrication, assembly, failure estimations of for ultra-thin chips stacking by using pre-molding technology. , 2015, , .		0
113	Development of simulation-approach for 3D chip stacking with fine-pitch array-type microbumps. , 2015, , .		0
114	Factorial designs of multi-coatings for induced stresses of advanced flexible displays. , 2016, , .		0
115	Accompanied arrangement effect of stretched gate width and dummy diffusion region on strained silicon PMOSFETs. , 2016, , .		0
116	Managing induced warpage of 3D-ICs packaging using multi-layered molding materials. , 2016, , .		0
117	Device layout effect of strained Ge-based NMOSFETs with Ge <sub>1-x</sub> Si <sub>x</sub> stressors. , 2016, , .		0
118	Shallow trench isolation geometric influence of a recessed surface on array-type arrangements of nano-scaled devices strained by contact etch stop liner and Ge-based stressors. Thin Solid Films, 2016, 618, 172-177.	1.8	0
119	Comprehensive effects of strained Ge <sub>1-x</sub> Sn <sub>x</sub> and device layout arrangement on a nano-scale Ge-based PMOSFET with a short channel. Materials Science in Semiconductor Processing, 2017, 70, 145-150.	4.0	0
120	Interaction influence of S/D GeSi lattice mismatch and stress gradient of CESL on nano-scaled strained nMOSFETs. Materials Science in Semiconductor Processing, 2017, 70, 254-259.	4.0	0
121	Effect of strained Ge-based NMOSFETs with Ge <sub>0.93</sub> Si <sub>0.07</sub> stressors on device layout. Solid-State Electronics, 2017, 138, 113-118.	1.4	0
122	The achievement of the super short channel control in the magnetic Ge n-FinFETs with the negative capacitance effect. Vacuum, 2017, 140, 63-65.	3.5	0
123	Effect of contact-etch-stop-layer and Si <sub>1-x</sub> Ge <sub>x</sub> channel mechanical properties on nano-scaled short channel NMOSFETs with dummy gate arrays. Microelectronics Reliability, 2018, 83, 230-234.	1.7	0
124	Magnifying the effective intrinsic stress of surface coating on the performance of nano-scaled Ge-based high-k/metal gate device through superficial layout designs. Thin Solid Films, 2018, 660, 725-729.	1.8	0
125	Laminated process effect of high-density redistributed trace lines on the risk estimation of induced-stress failure for 3D-IC embedded interposer. Microsystem Technologies, 2019, 25, 2021-2028.	2.0	0
126	Design and Validation of Reliability Physics for Interconnect Architectures Induced from Inclusive TM/SM/EM Effects. , 2020, , .		0



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127	Interactive Field Effect of Atomic Bonding Forces on the Equivalent Elastic Modulus Estimation of Micro-Level Single-Crystal Copper by Utilizing Atomistic-Continuum Finite Element Simulation. Molecules, 2020, 25, 5107.	3.8	0
128	Thermal Stress-Induced Interfacial Failure Modes of Advanced Electronic Devices. , 2014, , 5495-5495.		0
129	Low Temperature SLID Bonding Approach in Fine Pitch Chip-stacking Structure with 30 $\mu$ m-pitch Interconnections. Transactions of the Japan Institute of Electronics Packaging, 2020, 13, E20-010-1-E20-010-4.	0.4	0
130	Microscopic mechanical simulation and experimental demonstration of deformed-induced failure for Li-ion battery package in electric vehicle. Mechanics of Advanced Materials and Structures, 2023, 30, 2341-2352.	2.6	0
131	Characteristic Analysis of a Multi-chip Embedded Interposer Carrier using a Wafer-Level Fan-Out Process. , 2022, , .		0