Susmit Sarkar

List of Publications by Year
in descending order

34 papers	2,162 citations	687363 13 h-index	839539 18 g-index
34 all docs	34 docs citations	34 times ranked	440 citing authors

#	Article	IF	Citations
1	x86-TSO. Communications of the ACM, 2010, 53, 89-97.	4.5	327
2	A Better x86 Memory Model: x86-TSO. Lecture Notes in Computer Science, 2009, , 391-407.	1.3	275
3	Mathematizing C++ concurrency. , 2011, , .		217
4	Understanding POWER multiprocessors. , 2011, , .		159
5	Fences in Weak Memory Models. Lecture Notes in Computer Science, 2010, , 258-272.	1.3	106
6	Ott: Effective tool support for the working semanticist. Journal of Functional Programming, 2010, 20, 71-122.	0.8	99
7	Simplifying ARM concurrency: multicopy-atomic axiomatic and operational models for ARMv8. , 2018, 2, 1-29.		87
8	Modelling the ARMv8 architecture, operationally: concurrency and ISA. , 2016, , .		85
9	An Axiomatic Memory Model for POWER Multiprocessors. Lecture Notes in Computer Science, 2012, , 495-512.	1.3	82
10	The semantics of x86-CC multiprocessor machine code. , 2009, , .		80
11	Clarifying and compiling C/C++ concurrency. , 2012, , .		77
12	Mathematizing C++ concurrency. ACM SIGPLAN Notices, 2011, 46, 55-66.	0.2	75
13	Synchronising C/C++ and POWER. , 2012, , .		67
14	The semantics of power and ARM multiprocessor machine code. , 2009, , .		65
15	Litmus: Running Tests against Hardware. Lecture Notes in Computer Science, 2011, , 41-44.	1.3	55
16	Understanding POWER multiprocessors. ACM SIGPLAN Notices, 2011, 46, 175-186.	0.2	45
17	The semantics of x86-CC multiprocessor machine code. ACM SIGPLAN Notices, 2009, 44, 379-391.	0.2	42
18	Ott. , 2007, , .		40

#	Article	IF	Citations
19	An integrated concurrency and core-ISA architectural envelope definition, and test oracle, for IBM POWER multiprocessors. , 2015, , .		27
20	Ott. ACM SIGPLAN Notices, 2007, 42, 1-12.	0.2	26
21	Nitpicking c++ concurrency. , 2011, , .		25
22	Fences in weak memory models (extended version). Formal Methods in System Design, 2012, 40, 170-205.	0.8	24
23	Modelling the ARMv8 architecture, operationally: concurrency and ISA. ACM SIGPLAN Notices, 2016, 51, 608-621.	0.2	19
24	Mixed-size concurrency: ARM, POWER, C/C++11, and SC. , 2017, , .		19
25	Clarifying and compiling C/C++ concurrency. ACM SIGPLAN Notices, 2012, 47, 509-520.	0.2	14
26	Synchronising C/C++ and POWER. ACM SIGPLAN Notices, 2012, 47, 311-322.	0.2	8
27	Automatically deriving cost models for structured parallel processes using hylomorphisms. Future Generation Computer Systems, 2018, 79, 653-668.	7.5	6
28	Mixed-size concurrency: ARM, POWER, C/C++11, and SC. ACM SIGPLAN Notices, 2017, 52, 429-442.	0.2	5
29	Foundational certified code in the Twelf metalogical framework. ACM Transactions on Computational Logic, 2008, 9, 1-26.	0.9	4
30	Fence placement for legacy data-race-free programs via synchronization read detection. , 2015, , .		1
31	Fence Placement for Legacy Data-Race-Free Programs via Synchronization Read Detection. Transactions on Architecture and Code Optimization, 2016, 12, 1-23.	2.0	1
32	Fence placement for legacy data-race-free programs via synchronization read detection. ACM SIGPLAN Notices, 2015, 50, 249-250.	0.2	0
33	Fast RMWs for TSO. ACM SIGPLAN Notices, 2013, 48, 61-72.	0.2	0
34	Timing Properties and Correctness for Structured Parallel Programs on x86-64 Multicores. Lecture Notes in Computer Science, 2016, , 101-125.	1.3	0