Mohamed Hassan

List of Publications by Year
in descending order

21 papers	254 citations	1478505 6 h-index	1474206 9 g-index
21 all docs	21 docs citations	21 times ranked	97 citing authors

#	Article	IF	Citations
1	A framework for scheduling DRAM memory accesses for multi-core mixed-time critical systems. , 2015, , .		43
2	Bounding DRAM Interference in COTS Heterogeneous MPSoCs for Mixed Criticality Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2323-2336.	2.7	31
3	Criticality- and Requirement-Aware Bus Arbitration for Multi-Core Mixed Criticality Systems. , 2016, , .		30
4	A Comparative Study of Predictable DRAM Controllers. Transactions on Embedded Computing Systems, 2018, 17, 1-23.	2.9	19
5	On the Off-Chip Memory Latency of Real-Time Systems: Is DDR DRAM Really the Best Option?. , 2018, , .		18
6	Predictable Cache Coherence for Multi-core Real-Time Systems. , 2017, , .		17
7	Heterogeneous MPSoCs for Mixed-Criticality Systems: Challenges and Opportunities. IEEE Design and Test, 2018, 35, 47-55.	1.2	16
8	PMC. Transactions on Embedded Computing Systems, 2017, 16, 1-28.	2.9	14
9	Reverse-engineering embedded memory controllers through latency-based analysis. , 2015, , .		12
10	Enabling Predictable, Simultaneous and Coherent Data Sharing in Mixed Criticality Systems. , 2019, , .		11
11	Designing Predictable Cache Coherence Protocols for Multi-Core Real-Time Systems. IEEE Transactions on Computers, 2021, 70, 2098-2111.	3.4	10
12	DRAMbulism: Balancing Performance and Predictability through Dynamic Pipelining. , 2020, , .		9
13	MCXplore: Automating the Validation Process of DRAM Memory Controller Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, , 1-1.	2.7	6
14	Reduced latency DRAM for multi-core safety-critical real-time systems. Real-Time Systems, 2020, 56, 171-206.	1.3	6
15	MCsim: An Extensible DRAM Memory Controller Simulator. IEEE Computer Architecture Letters, 2020, 19, 105-109.	1.5	6
16	MCXplore: An Automated Framework for Validating Memory Controller Designs. , 2016, , .		2
17	DuoMC: Tight DRAM Latency Bounds with Shared Banks and Near-COTS Performance. , 2021, , .		2
18	Exposing Implementation Details of Embedded DRAM Memory Controllers through Latency-based Analysis. Transactions on Embedded Computing Systems, 2018, 17, 1-25.	2.9	1

#	Article	IF	Citations
19	Demystifying the Characteristics of High Bandwidth Memory for Real-Time Systems. , 2021, , .		1
20	Managing DRAM Interference in Mixed Criticality Embedded Systems. , 2019, , .		0
21	Duetto: Latency Guarantees at Minimal Performance Cost. , 2021, , .		0