Vinod Pangracious

List of Publications by Year
in descending order

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40	118	1683354 5	1473754 9
papers	citations	h-index	g-index

44	44	44	119
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Blockchain Based Energy Trade. , 2022, , .		1
2	A Decentralized Autonomous Ecosystem for Peer-To-Peer Clean Energy Trade. , 2020, , .		0
3	Advanced Operation for Micro-Grid on Residential Properties for Network Power Stability During Peak Load. , 2019, , .		1
4	ATAR: An Adaptive Thermal-Aware Routing Algorithm for 3-D Network-on-Chip Systems. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2018, 8, 2122-2129.	1.4	11
5	A Bio-Inspired Hybrid Thermal Management Approach for 3-D Network-on-Chip Systems. IEEE Transactions on Nanobioscience, 2017, 16, 727-743.	2.2	8
6	A review of feature extraction for EEG epileptic seizure detection and classification. , 2017, , .		26
7	Thermal Management in 3D Homogeneous NoC Systems Using Optimized Placement of Liquid Microchannels. , 2017, , .		0
8	An efficient multi-objective thermal aware routing algorithm 3D network-on-chips. , 2017, , .		3
9	Performance analysis and optimization of cluster-based mesh FPGA architectures: design methodology and CAD tool support. Turkish Journal of Electrical Engineering and Computer Sciences, 2017, 25, 2044-2054.	0.9	0
10	Novel Three-Dimensional Embedded FPGA Technology and Achitecture. Computer Architecture News, 2017, 44, 50-55.	2.5	0
11	Artifical immune system using Genetic Algorithm and decision tree. , 2016, , .		0
12	Exploration of Mesh-Based FPGA Architecture: Comparison of 2D and 3D Technologies in Terms of Power, Area and Performance. , 2016, , .		2
13	Improvement of cluster-based Mesh FPGA architecture using novel hierarchical interconnect topology and long routing wires. Microprocessors and Microsystems, 2016, 40, 16-26.	1.8	5
14	An efficient Mesh-of-Tree based interconnect architecture for high performance 3D FPGAs. , 2015, , .		0
15	Design and Optimization of a Horizontally Partitioned, High-Speed, 3D Tree-Based FPGA. IEEE Micro, 2015, 35, 48-59.	1.8	0
16	Three-Dimensional Tree-Based FPGA: Architecture Exploration Tools and Technologies. Lecture Notes in Electrical Engineering, 2015, , 117-146.	0.3	0
17	Three-Dimensional Integration: A More Than Moore Technology. Lecture Notes in Electrical Engineering, 2015, , 13-41.	0.3	8
18	Three-Dimensional Design Methodologies for Tree-based FPGA Architecture. Lecture Notes in Electrical Engineering, 2015, , .	0.3	2

#	Article	IF	Citations
19	Mesh of Clusters FPGA Architectures: Exploration Methodology and Interconnect Optimization. Lecture Notes in Computer Science, 2015, , 411-418.	1.0	3
20	Three-Dimensional FPGAs: Configuration and CAD Development. Lecture Notes in Electrical Engineering, 2015, , 95-116.	0.3	0
21	Three-Dimensional FPGAs: Future Lines of Research. Lecture Notes in Electrical Engineering, 2015, , 201-209.	0.3	0
22	Field Programmable Gate Arrays: An Overview. Lecture Notes in Electrical Engineering, 2015, , 43-71.	0.3	1
23	Three-dimensional Mesh of Clusters: An alternative unified high performance interconnect architecture for 3D-FPGA implementation. , 2014, , .		2
24	On wiring delays reduction of tree-based FPGA using 3-D fabric. , 2014, , .		0
25	Exploration and optimization of heterogeneous interconnect fabric of 3D tree-based FPGA. , 2014, , .		0
26	Architecture level optimization of 3-dimensional tree-based FPGA. Microelectronics Journal, 2014, 45, 355-366.	1.1	1
27	Designing 3D tree-based FPGA: Interconnect optimization and thermal analysis. , 2013, , .		0
28	Design and optimization of heterogeneous tree-based FPGA using 3D technology. , 2013, , .		0
29	TSV count minimization and thermal analysis for 3D Tree-based FPGA. , 2013, , .		1
30	Designing a 3D tree-based FPGA: Optimization of butterfly programmable interconnect topology using 3D technology. , 2013, , .		5
31	Exploration environment for 3D heterogeneous tree-based FPGA architectures (3D HT-FPGA). , 2013, , .		1
32	Physical design exploration of 3D tree-based FPGA architecture. , 2013, , .		2
33	High performance 3-dimensional heterogeneous tree-based FPGA architectures (HT-FPGA). , 2013, , .		0
34	Architecture level TSV count minimization methodology for 3D tree-based FPGA. , 2013, , .		0
35	Performance Analysis and Optimization of High Density Tree-Based 3D Multilevel FPGA. Lecture Notes in Computer Science, 2013, , 197-209.	1.0	9
36	PROJECT HAWK: An innovative introduction of practical learning and entrepreneurship in engineering education. , 2012, , .		3

#	Article	IF	Citations
37	Design & implementation of configurable logic block (CLB) using SET based QCA technology. , 2012, , .		0
38	Design & implementation of configurable logic block (CLB) using SET based QCA technology. , 2012, , .		0
39	A Comparative Study of Placement of Processor on Silicon and Thermal Analysis. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2012, , 654-662.	0.2	0
40	Through Silicon Via-Based Grid for Thermal Control in 3D Chips. Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering, 2009, , 90-98.	0.2	21