Ayan Banerjee

List of Publications by Year
in descending order

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16	45	2258059	1872680
papers	citations	3 h-index	6 g-index

16	16	16	25
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Pipelined VLSI Architecture using CORDIC for Transform Domain Equalizer. Journal of Signal Processing Systems, 2013, 70, 39-48.	2.1	9
2	A memory and area-efficient distributed arithmetic based modular VLSI architecture of 1D/2D reconfigurable 9/7 and 5/3 DWT filters for real-time image decomposition. Journal of Real-Time Image Processing, 2020, 17, 1421-1446.	3.5	8
3	Optimal Image Fusion Algorithm using Modified Grey Wolf Optimization amalgamed with Cuckoo Search, Levy Fly and Mantegna Algorithm. , 2020, , .		5
4	Low Latency Semi-iterative CORDIC Algorithm using Normalized Angle Recoding and its VLSI Implementation. , 2019, , .		4
5	CORDIC-Based High-Speed VLSI Architecture of Transform Model Estimation for Real-Time Imaging. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 215-226.	3.1	3
6	A systematic approach for the design of linear filters and oscillators employing tree representation. Analog Integrated Circuits and Signal Processing, 2021, 108, 181-203.	1.4	3
7	Cell-based Coherent Design Methodology for Linear and Non-linear Analog Circuits. , 2019, , .		2
8	Optimal Image Fusion Algorithm using Modified Whale Optimization Algorithm Amalgamed with Local Search and BAT Algorithm. , 2020, , .		2
9	Area and memory efficient tunable VLSI implementation of DWT filters for image decomposition using distributed arithmetic. International Journal of Electronics, 2020, 107, 1913-1939.	1.4	2
10	A Memory Efficient, Multiplierless & Modular VLSI Architecture of 1D/2D Re-Configurable 9/7 & 5/3 DWT Filters Using Distributed Arithmetic. Journal of Circuits, Systems and Computers, 2020, 29, 2050151.	1.5	2
11	A Novel Paradigm of CORDIC-Based FFT Architecture Framed on the Optimality of High-Radix Computation. Circuits, Systems, and Signal Processing, 2021, 40, 311-334.	2.0	2
12	VLSI Architecture of Sigmoid Activation Function for Rapid Prototyping of Machine Learning Applications. , 2021, , .		2
13	Low Area & Memory Efficient VLSI Architecture of 1D/2D DWT for Real Time Image Decomposition. , 2018, , .		1
14	Analog VLSI Design of Current-Mode DCT for 1-D Signal Processing. , 2019, , .		0
15	A Novel Reconfigurable Analog VLSI Architecture of M-point DFT Using Complex Matrix Multiplier and Graph-Based Signal Routing Method. Circuits, Systems, and Signal Processing, 0, , .	2.0	0
16	Systematic realization of non-linear arithmetic functions using hexagonal Field Programmable Analog Array. Microelectronics Journal, 2022, 126, 105495.	2.0	0