Sara Choi

List of Publications by Year
in descending order

8	68	1684188 5	1872680 6
papers	citations	h-index	g-index

8	8	8	69
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Self-Referenced Single-Ended Resistance Monitoring Write Termination Scheme for STT-RAM Write Energy Reduction. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 2481-2493.	5.4	3
2	Area- and Energy-Efficient STDP Learning Algorithm for Spiking Neural Network SoC. IEEE Access, 2020, 8, 216922-216932.	4.2	8
3	Offset-Canceling Single-Ended Sensing Scheme With One-Bit-Line Precharge Architecture for Resistive Nonvolatile Memory in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2548-2555.	3.1	12
4	Offset-Cancellation Sensing-Circuit-Based Nonvolatile Flip-Flop Operating in Near-Threshold Voltage Region. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2963-2972.	5.4	15
5	A Decoder for Short BCH Codes With High Decoding Efficiency and Low Power for Emerging Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 387-397.	3.1	16
6	Evaluation of STT-MRAM L3 cache in 7nm FinFET process. , 2018, , .		6
7	Area-optimal sensing circuit designs in deep submicrometer STT-RAM. , 2016, , .		3
8	Corner-Aware Dynamic Gate Voltage Scheme to Achieve High Read Yield in STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2851-2860.	3.1	5