Ali Azarpeyvand

List of Publications by Year
in descending order

26	113	1684188 5	1588992 8
papers	citations	h-index	g-index

27	27	27	89
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Data-Driven and Knowledge-Based Algorithms for Gene Network Reconstruction on High-Dimensional Data. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2022, 19, 1545-1557.	3.0	2
2	Significantly improving human detection in low-resolution images by retraining YOLOv3. , 2021, , .		1
3	Hardware Implementation of a Chaos Based Image Encryption Using High-Level Synthesis. , 2021, , .		0
4	Vulnerability Analysis of Adder Architectures Considering Design and Synthesis Constraints. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 7-14.	1.2	2
5	Towards memristor-based approximate accelerator: application to complex-valued FIR filter bank. Analog Integrated Circuits and Signal Processing, 2018, 96, 577-588.	1.4	4
6	Code Acceleration Using Memristor-Based Approximate Matrix Multiplier: Application to Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2684-2695.	3.1	16
7	Parallel Algorithms for Inferring Gene Regulatory Networks: A Review. Current Genomics, 2018, 19, 603-614.	1.6	6
8	Memristor-based approximate matrix multiplier. Analog Integrated Circuits and Signal Processing, 2017, 93, 363-373.	1.4	8
9	An ultra-fast multi-objective optimization algorithm for VLIW architecture. , 2016, , .		0
10	Reliability aware throughput management of chip multi-processor architecture via thread migration. Journal of Supercomputing, 2016, 72, 1363-1380.	3.6	6
11	Fast and accurate architectural vulnerability analysis for embedded processors using Instruction Vulnerability Factor. Microprocessors and Microsystems, 2016, 42, 113-126.	2.8	7
12	Reliabilityâ€aware simultaneous multithreaded architecture using online architectural vulnerability factor estimation. IET Computers and Digital Techniques, 2015, 9, 124-133.	1.2	3
13	An analytical method for reliability aware instruction set extension. Journal of Supercomputing, 2014, 67, 104-130.	3.6	3
14	Reliability-aware cross-layer custom instruction screening. , 2013, , .		2
15	A novel hardware implementation for the IEEE 802.22 Turbo-Like Interleaver. , 2012, , .		0
16	Vulnerability Analysis for Custom Instructions. , 2012, , .		6
17	CIVA: Custom instruction vulnerability analysis framework. , 2012, , .		6
18	Hardware implementation of the bit interleaver for the IEEE 802.22 Standard. , 2012, , .		0

#	Article	IF	Citations
19	Adaptive fault-tolerant DVFS with dynamic online AVF prediction. Microelectronics Reliability, 2012, 52, 1197-1208.	1.7	6
20	Reliability considerations in dynamic voltage and frequency scaling schemes. , 2010, , .		2
21	Energy/throughput trade-off in a fully asynchronous NoC for GALS-based MPSoC architectures. , 2010, , .		5
22	Instruction reliability analysis for embedded processors. , 2010, , .		14
23	Reliability Analysis of Embedded Applications in Non-Uniform Fault Tolerant Processors. , 2010, , .		2
24	Analysis of single-event effects in embedded processors for non-uniform fault tolerant design. , 2009, , .		2
25	Reduced-Memory Direct Digital Frequency Synthesizer Using Parabolic Initial Guess. Analog Integrated Circuits and Signal Processing, 2003, 34, 89-96.	1.4	5
26	A novel architecture for sine-output direct digital frequency synthesizers using parabolic approximation. , 0, , .		5