

Ali Azarpeyvand

List of Publications by Year in descending order

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Version: 2024-02-01

26
papers

113
citations

1684188

5
h-index

1588992

8
g-index

27
all docs

27
docs citations

27
times ranked

89
citing authors

#	ARTICLE	IF	CITATIONS
1	Code Acceleration Using Memristor-Based Approximate Matrix Multiplier: Application to Convolutional Neural Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2684-2695.	3.1	16
2	Instruction reliability analysis for embedded processors. , 2010, , .		14
3	Memristor-based approximate matrix multiplier. Analog Integrated Circuits and Signal Processing, 2017, 93, 363-373.	1.4	8
4	Fast and accurate architectural vulnerability analysis for embedded processors using Instruction Vulnerability Factor. Microprocessors and Microsystems, 2016, 42, 113-126.	2.8	7
5	Vulnerability Analysis for Custom Instructions. , 2012, , .		6
6	CIVA: Custom instruction vulnerability analysis framework. , 2012, , .		6
7	Adaptive fault-tolerant DVFS with dynamic online AVF prediction. Microelectronics Reliability, 2012, 52, 1197-1208.	1.7	6
8	Reliability aware throughput management of chip multi-processor architecture via thread migration. Journal of Supercomputing, 2016, 72, 1363-1380.	3.6	6
9	Parallel Algorithms for Inferring Gene Regulatory Networks: A Review. Current Genomics, 2018, 19, 603-614.	1.6	6
10	A novel architecture for sine-output direct digital frequency synthesizers using parabolic approximation. , 0, , .		5
11	Reduced-Memory Direct Digital Frequency Synthesizer Using Parabolic Initial Guess. Analog Integrated Circuits and Signal Processing, 2003, 34, 89-96.	1.4	5
12	Energy/throughput trade-off in a fully asynchronous NoC for GALS-based MPSoC architectures. , 2010, , .		5
13	Towards memristor-based approximate accelerator: application to complex-valued FIR filter bank. Analog Integrated Circuits and Signal Processing, 2018, 96, 577-588.	1.4	4
14	An analytical method for reliability aware instruction set extension. Journal of Supercomputing, 2014, 67, 104-130.	3.6	3
15	Reliability-aware simultaneous multithreaded architecture using online architectural vulnerability factor estimation. IET Computers and Digital Techniques, 2015, 9, 124-133.	1.2	3
16	Analysis of single-event effects in embedded processors for non-uniform fault tolerant design. , 2009, , .		2
17	Reliability considerations in dynamic voltage and frequency scaling schemes. , 2010, , .		2
18	Reliability Analysis of Embedded Applications in Non-Uniform Fault Tolerant Processors. , 2010, , .		2

#	ARTICLE	IF	CITATIONS
19	Reliability-aware cross-layer custom instruction screening. , 2013, , .		2
20	Vulnerability Analysis of Adder Architectures Considering Design and Synthesis Constraints. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 7-14.	1.2	2
21	Data-Driven and Knowledge-Based Algorithms for Gene Network Reconstruction on High-Dimensional Data. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2022, 19, 1545-1557.	3.0	2
22	Significantly improving human detection in low-resolution images by retraining YOLOv3. , 2021, , .		1
23	A novel hardware implementation for the IEEE 802.22 Turbo-Like Interleaver. , 2012, , .		0
24	Hardware implementation of the bit interleaver for the IEEE 802.22 Standard. , 2012, , .		0
25	An ultra-fast multi-objective optimization algorithm for VLIW architecture. , 2016, , .		0
26	Hardware Implementation of a Chaos Based Image Encryption Using High-Level Synthesis. , 2021, , .		0