

# Massimo Alioto

## List of Publications by Year in descending order

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123  
papers

2,932  
citations

186265

28  
h-index

197818

49  
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126  
all docs

126  
docs citations

126  
times ranked

1746  
citing authors

#	ARTICLE	IF	CITATIONS
1	In-Memory Unified TRNG and Multi-Bit PUF for Ubiquitous Hardware Security. IEEE Journal of Solid-State Circuits, 2022, 57, 153-166.	5.4	18
2	Editorial Opening of the 2022 TVLSI Editorial Yearâ€™Connecting Trends From Society to VLSI Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 1-4.	3.1	1
3	STT-BNN: A Novel STT-MRAM In-Memory Computing Macro for Binary Neural Networks. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2022, 12, 569-579.	3.6	22
4	Sub-nW Microcontroller With Dual-Mode Logic and Self-Startup for Battery-Indifferent Sensor Nodes. IEEE Journal of Solid-State Circuits, 2021, 56, 1618-1629.	5.4	12
5	On-Chip Links With Energy-Quality Tradeoff in Error-Resilient and Machine Learning Applications. IEEE Journal of Solid-State Circuits, 2021, , 1-1.	5.4	0
6	Rail-to-Rail Dynamic Voltage Comparator Scalable Down to pW-Range Power and 0.15-V Supply. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 2675-2679.	3.0	17
7	Opening of the 2021 Editorial Yearâ€™Overture for a New Year of Change. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1-2.	3.1	2
8	A Robust, High-Speed and Energy-Efficient Ultralow-Voltage Level Shifter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1393-1397.	3.0	13
9	STT-MRAM Architecture with Parallel Accumulator for In-Memory Binary Neural Networks. , 2021, , .		5
10	Second Quarter of the 2021 Editorial Yearâ€™A Year in Crescendo. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 815-842.	3.1	1
11	PUF Architecture with Run-Time Adaptation for Resilient and Energy-Efficient Key Generation via Sensor Fusion. IEEE Journal of Solid-State Circuits, 2021, 56, 2182-2192.	5.4	10
12	Design of Digital OTAs With Operation Down to 0.3 V and nW Power for Direct Harvesting. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 3693-3706.	5.4	29
13	A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3073-3077.	3.0	16
14	A 0.6-to-1.8V CMOS Current Reference With Near-100% Power Utilization. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 3038-3042.	3.0	11
15	Â±CIM SRAM for Signed In-Memory Broad-Purpose Computing From DSP to Neural Processing. IEEE Journal of Solid-State Circuits, 2021, 56, 2981-2992.	5.4	18
16	Trimming-Less Voltage Reference for Highly Uncertain Harvesting Down to 0.25 V, 5.4 pW. IEEE Journal of Solid-State Circuits, 2021, 56, 3134-3144.	5.4	27
17	From Less Batteries to Battery-Less Alert Systems with Wide Power Adaptation down to nWsâ€™Toward a Smarter, Greener World. IEEE Design and Test, 2021, 38, 90-133.	1.2	19
18	Fully Synthesizable Unified True Random Number Generator and Cryptographic Core. IEEE Journal of Solid-State Circuits, 2021, 56, 3049-3061.	5.4	10

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19	A 3.2-pW, 0.2-V Trimming-Less Voltage Reference with 1.4-mV Across-Wafer Total Accuracy. , 2021, , .		3
20	SRAM with In-Memory Inference and 90% Bitline Activity Reduction for Always-On Sensing with 109 TOPS/mm <sup>2</sup> and 749-1,459 TOPS/W in 28nm. , 2021, , .		0
21	SRAM with In-Memory Inference and 90% Bitline Activity Reduction for Always-On Sensing with 109 TOPS/mm <sup>2</sup> and 749-1,459 TOPS/W in 28nm. , 2021, , .		0
22	TempDiff: Feature Map-Level CNN Sparsity Enhancement at Near-Zero Memory Overhead via Temporal Difference. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2021, 11, 620-633.	3.6	2
23	Automated Design of Reconfigurable Microarchitectures for Accelerators Under Wide-Voltage Scaling. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 777-790.	3.1	2
24	Editorial on the Opening of the New Editorial Yearâ€”The State of the IEEE Transactions on Very Large Scale Integration (VLSI) Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1-2.	3.1	1
25	Integrated Power Management for Battery-Indifferent Systems With Ultra-Wide Adaptation Down to nW. IEEE Journal of Solid-State Circuits, 2020, 55, 967-976.	5.4	19
26	Low-Energy Voice Activity Detection via Energy-Quality Scaling From Data Conversion to Machine Learning. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 1378-1388.	5.4	10
27	Fully Digital Rail-to-Rail OTA With Sub-1000- $\mu\text{m}^2$ Area, 250-mV Minimum Supply, and nW Power at 150-pF Load in 180 nm. IEEE Solid-State Circuits Letters, 2020, 3, 474-477.	2.0	35
28	Deep Sub-pJ/Bit Low-Area Energy-Security Scalable SIMON Crypto-Core in 40 nm. , 2020, , .		3
29	Fully Synthesizable All-Digital Unified Dynamic Entropy Generation, Extraction, and Utilization Within the Same Cryptographic Core. IEEE Solid-State Circuits Letters, 2020, 3, 402-405.	2.0	3
30	Broad-Purpose In-Memory Computing for Signal Monitoring and Machine Learning Workloads. IEEE Solid-State Circuits Letters, 2020, 3, 394-397.	2.0	11
31	Editorial on the Conclusion of the 2020 Editorial Yearâ€”The Climactic Finale of a Peculiar Year. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2479-2480.	3.1	0
32	Approximate Multipliers With Dynamic Truncation for Energy Reduction via Graceful Quality Degradation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 3427-3431.	3.0	13
33	Fully Synthesizable Low-Area Analogue-to-Digital Converters With Minimal Design Effort Based on the Dyadic Digital Pulse Modulation. IEEE Access, 2020, 8, 70890-70899.	4.2	35
34	Processor Energyâ€”Performance Range Extension Beyond Voltage Scaling via Drop-In Methodologies. IEEE Journal of Solid-State Circuits, 2020, 55, 2670-2679.	5.4	5
35	Adaptive Digital Circuits for Power-Performance Range beyond Wide Voltage Scaling. , 2020, , .		7
36	Energy-Quality Scalable Memory-Frugal Feature Extraction for Always-On Deep Sub-mW Distributed Vision. IEEE Access, 2020, 8, 18951-18961.	4.2	3

#	ARTICLE	IF	CITATIONS
37	Automated Design Flows and Run-Time Optimization for Reconfigurable Microarchitectures. , 2020, , 55-92.		0
38	Reconfigurable Clock Networks, Automated Design Flows, Run-Time Optimization, and Case Study. , 2020, , 115-144.		2
39	Voice Activity Detection with >83% Accuracy under SNR down to $\hat{\sim}3\text{dB}$ at $\$1.19\mu\text{m}^2\text{W}\$$ and $0.07\text{mm}^2$ in 40nm. , 2020, , .		1
40	Editorial: TVLSI Keynote Papers Enriching Our Transactions With Invited Contributions. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1485-1485.	3.1	0
41	Reconfigurable Clock Networks for Wide Voltage Scaling. IEEE Journal of Solid-State Circuits, 2019, 54, 2622-2631.	5.4	8
42	Low-Swing Links with Dynamic Energy-Quality Trade-off for Error-Resilient Applications. , 2019, , .		3
43	Trends in Hardware Security: From Basics to ASICs. IEEE Solid-State Circuits Magazine, 2019, 11, 56-74.	0.4	58
44	Enabling Ubiquitous Hardware Security via Energy-Efficient Primitives and Systems : (Invited Paper). , 2019, , .		11
45	Standard Cell-Based Ultra-Compact DACs in 40-nm CMOS. IEEE Access, 2019, 7, 126479-126488.	4.2	30
46	Editorial TVLSI Positioningâ€”Continuing and Accelerating an Upward Trajectory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 253-280.	3.1	6
47	Fully Synthesizable Low-Area Digital-to-Analog Converter With Graceful Degradation and Dynamic Power-Resolution Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2865-2875.	5.4	31
48	Fully-Synthesizable Current-Input ADCs for Ultra-Low Area and Minimal Design Effort. , 2019, , .		5
49	PUF-based Key Generation with Design Margin Reduction via In-Situ and PVT Sensor Fusion. , 2019, , .		1
50	Energy-Quality Scalable Analog-to-Digital Conversion and Machine Learning Engine in a 51.9 nJ/frame Voice Activity Detector. , 2019, , .		0
51	An Energy Aware Variation-Tolerant Writing Termination Control for STT-based Non Volatile Flip-Flops. , 2019, , .		2
52	Minimum-Effort Design of Ultra-Low Power Interfaces for the Internet of Things. , 2019, , .		3
53	A pW-Power Hz-Range Oscillator Operating With a $0.3\text{â€}1.8\text{-V}$ Unregulated Supply. IEEE Journal of Solid-State Circuits, 2019, 54, 1487-1496.	5.4	38
54	Token-Based Security for the Internet of Things With Dynamic Energy-Quality Tradeoff. IEEE Internet of Things Journal, 2019, 6, 2843-2859.	8.7	46

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55	Energy-Quality Scalable Adders Based on Nonzeroing Bit Truncation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 964-968.	3.1	20
56	Ultra-Low Power and Minimal Design Effort Interfaces for the Internet of Things: Invited paper. , 2019, , ,		3
57	Drop-In Energy-Performance Range Extension in Microcontrollers Beyond VDD Scaling. , 2019, , .		4
58	Dynamically Adaptable Pipeline for Energy-Efficient Microarchitectures Under Wide Voltage Scaling. IEEE Journal of Solid-State Circuits, 2018, 53, 632-641.	5.4	21
59	The Internet of Things on Its Edge: Trends Toward Its Tipping Point. IEEE Consumer Electronics Magazine, 2018, 7, 77-87.	2.3	63
60	A Variation-Aware Timing Modeling Approach for Write Operation in Hybrid CMOS/STT-MTJ Circuits. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1086-1095.	5.4	41
61	iRazor: Current-Based Error Detection and Correction Scheme for PVT Variation in 40-nm ARM Cortex-R4 Processor. IEEE Journal of Solid-State Circuits, 2018, 53, 619-631.	5.4	62
62	Dynamic Reference Voltage Sensing Scheme for Read Margin Improvement in STT-MRAMs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1269-1278.	5.4	26
63	Display Stream Compression Encoder Architectures for Real-time 4K and 8K Video Encoding. , 2018, , .		5
64	Guest Editorial Energy-Quality Scalable Circuits and Systems for Sensing and Computing: From Approximate to Communication-Inspired and Learning-Based. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 361-368.	3.6	11
65	Energy-Quality Scalable Integrated Circuits and Systems: Continuing Energy Scaling in the Twilight of Moore's Law. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2018, 8, 653-678.	3.6	29
66	Fully Synthesizable PUF Featuring Hysteresis and Temperature Compensation for 3.2% Native BER and 1.02 fJ/b in 40 nm. IEEE Journal of Solid-State Circuits, 2018, 53, 2828-2839.	5.4	70
67	Fully Synthesizable, Rail-to-Rail Dynamic Voltage Comparator for Operation down to 0.3 V. , 2018, , .		19
68	Time-Based Sensing for Reference-Less and Robust Read in STT-MRAM Memories. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3338-3348.	5.4	23
69	26.3 Reconfigurable clock networks for random skew mitigation from subthreshold to nominal voltage. , 2017, , .		5
70	Energy-quality scalable adaptive VLSI circuits and systems beyond approximate computing. , 2017, , .		30
71	A Novel Framework to Estimate the Path Delay Variability On the Back of an Envelope via the Fan-Out-of-4 Metric. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2073-2085.	5.4	21
72	Guest Editorial Special Issue on Circuits and Systems for the Internet of Things"From Sensing to Sensemaking. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 2221-2225.	5.4	10

#	ARTICLE	IF	CITATIONS
73	Design-Oriented Energy Models for Wide Voltage Scaling Down to the Minimum Energy Point. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3115-3125.	5.4	7
74	Power-precision scalable latch memories. , 2017, , .		8
75	A closed-form energy model for VLSI circuits under wide voltage scaling. , 2016, , .		3
76	8.8 iRazor: 3-transistor current-based error detection and correction in an ARM Cortex-R4 processor. , 2016, , .		52
77	Novel Boosted-Voltage Sensing Scheme for Variation-Resilient STT-MRAM Read. IEEE Transactions on Circuits and Systems I: Regular Papers, 2016, 63, 1652-1660.	5.4	28
78	Voltage Scaled STT-MRAMs Towards Minimum-Energy Write Access. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2016, 6, 305-318.	3.6	19
79	Static Physically Unclonable Functions for Secure Chip Identification With 1.9% Native Bit Instability at 0.6 V and 15 fJ/bit in 65 nm. IEEE Journal of Solid-State Circuits, 2016, 51, 763-775.	5.4	54
80	Approximate SRAMs With Dynamic Energy-Quality Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 2128-2141.	3.1	37
81	Jitter analysis and measurement in subthreshold source-coupled differential ring oscillators. , 2015, , .		0
82	Variations in Nanometer CMOS Flip-Flops: Part I – Impact of Process Variations on Timing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 2035-2043.	5.4	80
83	Variations in Nanometer CMOS Flip-Flops: Part II – Energy Variability and Impact of Other Sources of Variations. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 835-843.	5.4	23
84	SRAM for Error-Tolerant Applications With Dynamic Energy-Quality Management in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 1310-1323.	5.4	54
85	Novel Self-Body-Biasing and Statistical Design for Near-Threshold Circuits With Ultra Energy-Efficient AES as Case Study. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1390-1401.	3.1	36
86	Comparative evaluation of Tunnel-FET ultra-low voltage SRAM bitcell and impact of variations. , 2014, , .		0
87	Effectiveness of Leakage Power Analysis Attacks on DPA-Resistant Logic Styles Under Process Variations. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 429-442.	5.4	49
88	A 346 $\mu\text{m}^2$ VCO-Based, Reference-Free, Self-Timed Sensor Interface for Cubic-Millimeter Sensor Nodes in 28 nm CMOS. IEEE Journal of Solid-State Circuits, 2014, 49, 2462-2473.	5.4	25
89	13.8 A 32kb SRAM for error-free and error-tolerant applications with dynamic energy-quality management in 28nm CMOS. , 2014, , .		18
90	Comparative soft error evaluation of layout cells in FinFET technology. Microelectronics Reliability, 2014, 54, 2300-2305.	1.7	24

#	ARTICLE	IF	CITATIONS
91	Tunnel FETs for Ultra-Low Voltage Digital VLSI Circuits: Part II – Evaluation at Circuit Level and Design Perspectives. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2499-2512.	3.1	29
92	Tunnel FETs for Ultralow Voltage Digital VLSI Circuits: Part I – Device – Circuit Interaction and Evaluation at Device Level. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2488-2498.	3.1	58
93	Enhancing the Static Noise Margins by Upsizing Length for Ultra-Low Voltage/Power/Energy Gates. Journal of Low Power Electronics, 2014, 10, 137-148.	0.6	11
94	Reconfigurable Power Management Unit for Energy Reduction in Sleep-Active Transitions. IEEE Journal of Solid-State Circuits, 2013, 48, 1921-1932.	5.4	29
95	Introduction to the special issue on IEEE-NEWCAS 2012. Analog Integrated Circuits and Signal Processing, 2013, 77, 93-94.	1.4	0
96	Impact of High-Mobility Materials on the Performance of Near- and Sub-Threshold CMOS Logic Circuits. IEEE Transactions on Electron Devices, 2013, 60, 972-977.	3.0	9
97	Guest Editorial for the Special Issue on Ultra-Low-Voltage VLSI Circuits and Systems for Green Computing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 849-852.	3.0	16
98	Active RFID: Perpetual wireless communications platform for sensors. , 2012, , .		11
99	Understanding the Basic Advantages of Bulk FinFETs for Sub- and Near-Threshold Logic Circuits From Device Measurements. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 439-442.	3.0	33
100	A Simple Circuit Approach to Reduce Delay Variations in Domino Logic Gates. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 2292-2300.	5.4	44
101	Ultra-Low Power VLSI Circuit Design Demystified and Explained: A Tutorial. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 3-29.	5.4	334
102	From energy – delay metrics to constraints on the design of digital circuits. International Journal of Circuit Theory and Applications, 2012, 40, 815-834.	2.0	16
103	Tapered-Vth Approach for Energy-Efficient CMOS Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2698-2707.	5.4	6
104	Modeling strategies of the input admittance of RC interconnects for VLSI CAD tools. Microelectronics Journal, 2011, 42, 63-73.	2.0	4
105	Simple and accurate modeling of the output transition time in nanometer CMOS gates. International Journal of Circuit Theory and Applications, 2010, 38, 995-1012.	2.0	2
106	Optimization of the wire grid size for differential routing: Analysis and impact on the power-delay-area tradeoff. Microelectronics Journal, 2010, 41, 669-679.	2.0	3
107	A VARIABILITY-TOLERANT FEEDBACK TECHNIQUE FOR THROUGHPUT MAXIMIZATION OF TRBGs WITH PREDEFINED ENTROPY. Journal of Circuits, Systems and Computers, 2010, 19, 879-895.	1.5	14
108	Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1597-1607.	5.4	149

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109	Understanding the Effect of Process Variations on the Delay of Static and Domino Logic. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 697-710.	3.1	166
110	Analysis and Modeling of Energy Consumption in RLC Tree Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 278.	3.1	4
111	Improving Power-Delay Performance of Ultra-Low-Power Subthreshold SCL Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 127-131.	3.0	20
112	Power-Aware Design of Nanometer MCML Tapered Buffers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 16-20.	3.0	10
113	Very fast carry energy efficient computation based on mixed dynamic/transmission-gate full adders. Electronics Letters, 2007, 43, 707.	1.0	3
114	Mixed Full Adder topologies for high-performance low-power arithmetic circuits. Microelectronics Journal, 2007, 38, 130-139.	2.0	62
115	The Digital Tent Map: Performance Analysis and Optimized Design as a Low-Complexity Source of Pseudorandom Bits. IEEE Transactions on Instrumentation and Measurement, 2006, 55, 1451-1458.	4.7	36
116	Design of cascaded ECL gates with power constraint. Electronics Letters, 2006, 42, 211.	1.0	1
117	Energy consumption in RC tree circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006, 14, 452-461.	3.1	15
118	Power-delay optimization of D-latch/MUX source coupled logic gates. International Journal of Circuit Theory and Applications, 2005, 33, 65-86.	2.0	17
119	Modelling and design considerations on CML gates under high-current effects. International Journal of Circuit Theory and Applications, 2005, 33, 503-518.	2.0	4
120	An efficient implementation of PRNGs based on the digital sawtooth map. International Journal of Circuit Theory and Applications, 2004, 32, 615-627.	2.0	8
121	Analysis and comparison on full adder block in submicron technology. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 806-823.	3.1	165
122	Modelling of source-coupled logic gates. International Journal of Circuit Theory and Applications, 2002, 30, 459-477.	2.0	20
123	Power estimation in adiabatic circuits: a simple and accurate model. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2001, 9, 608-615.	3.1	25