Ming-Chang Yang

List of Publications by Year
in descending order

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57	492	1039406	1058022
papers	citations	9	14
		h-index	g-index

57	57	57	239
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Leveraging Write Heterogeneity of Phase Change Memory on Supporting Self-Balancing Binary Tree. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1757-1770.	1.9	3
2	A File-Oriented Fast Secure Deletion Strategy for Shingled Magnetic Recording Drives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2463-2476.	1.9	2
3	KVSTL: An Application Support to LSM-Tree Based Key-Value Store via Shingled Translation Layer Data Management. IEEE Transactions on Computers, 2022, 71, 1598-1611.	2.4	3
4	MAGIC: Making IMR-Based HDD Perform Like CMR-Based HDD. IEEE Transactions on Computers, 2022, 71, 643-657.	2.4	3
5	Performance Enhancement of SMR-Based Deduplication Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 2835-2848.	1.9	3
6	On Minimizing Internal Data Migrations of Flash Devices via Lifetime-Retention Harmonization. IEEE Transactions on Computers, 2021, 70, 428-439.	2.4	5
7	Optimizing Lifetime Capacity and Read Performance of Bit-Alterable 3-D NAND Flash. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2021, 40, 218-231.	1.9	3
8	Enabling the Duo-phase Data Management to Realize Longevity Bit-alterable Flash Memory. IEEE Transactions on Computers, 2021, , 1-1.	2.4	0
9	Move-On-Modify: An Efficient yet Crash-Consistent Update Strategy for Interlaced Magnetic Recording. , 2021, , .		1
10	Joint Management of CPU and NVDIMM for Breaking Down the Great Memory Wall. IEEE Transactions on Computers, 2020, 69, 722-733.	2.4	15
11	When Storage Response Time Catches Up With Overall Context Switch Overhead, What Is Next?. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4266-4277.	1.9	11
12	Shift-Limited Sort: Optimizing Sorting Performance on Skyrmion Memory-Based Systems. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 4115-4128.	1.9	8
13	Request Flow Coordination for Growing-Scale Solid-State Drives. IEEE Transactions on Computers, 2020, 69, 832-843.	2.4	0
14	Parallel-Log-Single-Compaction-Tree: Flash-Friendly Two-Level Key-Value Management in KVSSDs. , 2020, , .		1
15	Permutation-Write: Optimizing Write Performance and Energy for Skyrmion Racetrack Memory. , 2020, , .		6
16	On Improving the Write Responsiveness for Host-Aware SMR Drives. IEEE Transactions on Computers, 2019, 68, 111-124.	2.4	13
17	Enabling File-Oriented Fast Secure Deletion on Shingled Magnetic Recording Drives. , 2019, , .		5
18	A Representation Learning Framework for Property Graphs. , 2019, , .		26

#	Article	IF	Citations
19	The Best of Both Worlds. , 2019, , .		3
20	Sky-RAM: Skyrmionic Random Access Memory. IEEE Electron Device Letters, 2019, 40, 722-725.	2.2	7
21	Replanting Your Forest: NVM-friendly Bagging Strategy for Random Forest. , 2019, , .		9
22	Co-Optimizing Storage Space Utilization and Performance for Key-Value Solid State Drives. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 29-42.	1.9	6
23	A new sequential-write-constrained cache management to mitigate write amplification for SMR drives. , 2019, , .		6
24	wrJFS: A Write-Reduction Journaling File System for Byte-addressable NVRAM. IEEE Transactions on Computers, 2018, 67, 1023-1038.	2.4	12
25	Rethinking self-balancing binary search tree over phase change memory with write asymmetry. , 2018, , .		3
26	On Harmonizing Data Lifetime and Block Retention Time for Flash Devices. , 2018, , .		1
27	Improving Runtime Performance of Deduplication System with Host-Managed SMR Storage Drives. , 2018, , .		5
28	Hot-Spot Suppression for Resource-Constrained Image Recognition Devices With Nonvolatile Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2567-2577.	1.9	18
29	Improving runtime performance of deduplication system with host-managed SMR storage drives. , 2018, , .		4
30	Enhancing Flash Memory Reliability by Jointly Considering Write-back Pattern and Block Endurance. ACM Transactions on Design Automation of Electronic Systems, 2018, 23, 1-24.	1.9	3
31	Boosting the performance with a data-backup-free programming scheme for TLC-based SSDs. , 2018, , .		2
32	KVFTL: Optimization of storage space utilization for key-value-specific flash storage devices. , 2017, , .		6
33	Performance Evaluation of Host Aware Shingled Magnetic Recording (HA-SMR) Drives. IEEE Transactions on Computers, 2017, 66, 1932-1945.	2.4	31
34	Enabling Write-Reduction Strategy for Journaling File Systems over Byte-addressable NVRAM. , 2017, , .		19
35	xB+-Tree: Access-Pattern-Aware Cache-Line-Based Tree for Non-volatile Main Memory Architecture. , 2017, , .		1
36	Virtual persistent cache: Remedy the long latency behavior of host-aware shingled magnetic recording drives. , 2017, , .		12

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37	Utilization-Aware Self-Tuning Design for TLC Flash Storage Devices. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3132-3144.	2.1	9
38	Reducing Data Migration Overheads of Flash Wear Leveling in a Progressive Way. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1808-1820.	2.1	15
39	Multi-Grained Block Management to Enhance the Space Utilization of File Systems on PCM Storages. IEEE Transactions on Computers, 2016, 65, 1831-1845.	2.4	3
40	Virtual Flash Chips: Reinforcing the Hardware Abstraction Layer to Improve Data Recoverability of Flash Devices. IEEE Transactions on Computers, 2016, 65, 2872-2883.	2.4	5
41	Graceful Space Degradation: An Uneven Space Management for Flash Storage Devices. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1425-1434.	1.9	0
42	Capacity-Independent Address Mapping for Flash Storage Devices with Explosively Growing Capacity. IEEE Transactions on Computers, 2016, 65, 448-465.	2.4	7
43	Byte-Addressable Update Scheme to Minimize the Energy Consumption of PCM-Based Storage Systems. Transactions on Embedded Computing Systems, 2016, 15, 1-20.	2.1	3
44	Logical data packing for multi-chip flash-memory storage systems. , 2015, , .		1
45	Reliability-aware striping with minimized performance overheads for flash-based storage devices. , 2015, , .		0
46	Efficient Victim Block Selection for Flash Storage Devices. IEEE Transactions on Computers, 2015, 64, 3444-3460.	2.4	9
47	Virtual flash chips. , 2015, , .		7
48	PWL: A Progressive Wear Leveling to Minimize Data Migration Overheads for NAND Flash Devices. , 2015, , .		9
49	Garbage collection and wear leveling for flash memory: Past and future. , 2014, , .		57
50	Endurance-aware clustering-based mining algorithm for non-volatile phase-change memory. , 2014, , .		2
51	Bad page relaxation to prolong the lifetime of flash devices. , 2014, , .		1
52	New ERA. , 2013, , .		55
53	A reliability enhancement design under the flash translation layer for MLC-based flash-memory storage systems. Transactions on Embedded Computing Systems, 2013, 13, 1-28.	2.1	17
54	A fifty-percent rule to minimize the energy consumption of PCM-based storage systems. , 2013, , .		1

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55	Migration-based hybrid cache design for file systems over flash storage devices. ACM SIGAPP Applied Computing Review: A Publication of the Special Interest Group on Applied Computing, 2013, 13, 8-16.	0.5	0
56	Performance enhancement of garbage collection for flash storage devices. , 2013, , .		22
57	Working-set-based address mapping for ultra-large-scaled flash devices. , 2012, , .		13