Shun-Ichiro Ohmi

List of Publications by Year
in descending order

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51	362	933447	1058476
papers	citations	10	14
		h-index	g-index

51	51	51	185
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Advanced gate dielectric materials for sub-100 nm CMOS. , 0, , .		48
2	Effect of ultrathin Mo and MoSix layer on Ti silicide reaction. Journal of Applied Physics, 1999, 86, 3655-3660.	2.5	22
3	Excellent Current Drivability and Environmental Stability in Room-Temperature-Fabricated Pentacene-Based Organic Field-Effect Transistors With ${m HfO}_{2}$ Gate Insulators. IEEE Transactions on Electron Devices, 2014, 61, 569-575.	3.0	18
4	Importance of Si surface flatness to realize high-performance Si devices utilizing ultrathin films with new material system. IEICE Electronics Express, 2014, 11, 20142006-20142006.	0.8	18
5	Hafnium-nitride gate insulator formed by electron-cyclotron-resonance plasma sputtering. IEICE Electronics Express, 2012, 9, 1329-1334.	0.8	14
6	Ferroelectric properties of undoped HfO₂ directly deposited on Si substrates by RF magnetron sputtering. Japanese Journal of Applied Physics, 2018, 57, 11UF09.	1.5	14
7	Impact of Si surface roughness on MOSFET characteristics with ultrathin HfON gate insulator formed by ECR plasma sputtering. IEICE Electronics Express, 2013, 10, 20130651-20130651.	0.8	13
8	Variability Improvement by Si Surface Flattening of Electrical Characteristics in MOSFETs With High-k HfON Gate Insulator. IEEE Transactions on Semiconductor Manufacturing, 2015, 28, 266-271.	1.7	13
9	Potential of MISFET with HfN gate dielectric formed by ECR plasma sputtering. Electronics Letters, 2013, 49, 500-501.	1.0	12
10	Investigation of bilayer HfN_x gate insulator utilizing ECR plasma sputtering. IEICE Electronics Express, 2016, 13, 20160054-20160054.	0.8	12
11	In-situ formation of Hf-based MONOS structures for non-volatile memory applications. IEICE Electronics Express, 2015, 12, 20150969-20150969.	0.8	11
12	Effect of Kr/O₂-Plasma Reactive Sputtering on Ferroelectric Nondoped HfOâ‚‚ Formation for MFSFET With Pt Gate Electrode. IEEE Transactions on Electron Devices, 2021, 68, 2427-2433.	3.0	11
13	Improvement of Endurance Characteristics for Al-Gate Hf-Based MONOS Structures on Atomically Flat Si(100) Surface Realized by Annealing in Ar/H₂ Ambient. IEICE Transactions on Electronics, 2018, E101.C, 328-333.	0.6	10
14	In situ formation of Hf-based metal/oxide/nitride/oxide/silicon structure for nonvolatile memory application. Japanese Journal of Applied Physics, 2018, 57, 114201.	1.5	10
15	Impact of Kr gas mixing in oxygen plasma etching of ferroelectric poly(vinylidene) Tj ETQq1 1 0.784314 rgBT /Overlock 10 Tf 50 182 Td	3.3	8
16	A study on precise control of PtSi work function by alloying with Hf. IEICE Electronics Express, 2011, 8, 45-49.	0.8	8
17	Contact resistivity reduction for PtSi/Si(100) by dopant segregation process. IEICE Electronics Express, 2013, 10, 20130778-20130778.	0.8	8
18	The Effect of PMA with TiN Gate Electrode on the Formation of Ferroelectric Undoped HfO₂ Directly Deposited on Si(100). IEICE Transactions on Electronics, 2019, E102.C, 435-440.	0.6	8

#	Article	IF	Citations
19	Low contact resistivity of barrier height controlled PtHfSi to Si evaluated by cross-bridge Kelvin resistor. IEICE Electronics Express, 2011, 8, 1710-1715.	0.8	7
20	Work function modulation of PtSi by alloying with Yb. IEICE Electronics Express, 2011, 8, 33-37.	0.8	7
21	The influence of Hf interlayers for ferroelectric non-doped HfO2 with suppressing the interfacial layer formation. Japanese Journal of Applied Physics, 2019, 58, SIIB16.	1.5	7
22	Ferroelectric Gate Field-Effect Transistors with 10nm Thick Nondoped HfO₂ Utilizing Pt Gate Electrodes. IEICE Transactions on Electronics, 2020, E103.C, 280-285.	0.6	7
23	Si Surface Orientation Dependence on the Electrical Characteristics of HfN Gate Insulator with sub-0.5 nm EOT Formed by ECR Plasma Sputtering. Materials Research Society Symposia Proceedings, 2014, 1588, 1.	0.1	6
24	Ferroelectric HfO₂ formation by annealing of a HfO₂/Hf/HfO₂/Si(100) stacked structure. Japanese Journal of Applied Physics, 2019, 58, SBBB08.	1.5	6
25	Fully Room-Temperature-Fabricated Low-Voltage Operating Pentacene-Based Organic Field-Effect Transistors With HfON Gate Insulator. IEEE Electron Device Letters, 2011, 32, 1600-1602.	3.9	5
26	Performance improvement of pentacene based organic field-effect transistor with HfON gate insulator. IEICE Electronics Express, 2011, 8, 1461-1466.	0.8	5
27	Experimental demonstration of a ferroelectric FET using paper substrate. IEICE Electronics Express, 2014, 11, 20140447-20140447.	0.8	5
28	Improvement of Hf-based metal/oxide/nitride/oxide/Si nonvolatile memory characteristics by Si surface atomically flattening. Japanese Journal of Applied Physics, 2020, 59, SGGB10.	1.5	5
29	Investigation of PDA process to improve electrical characteristics of HfO<inf>x</inf>N<inf>y</inf> High-k dielectric formed by ECR plasma oxidation of HfN. , 2007, , .		4
30	Selective etching of HfN gate electrode for HfN/HfSiON gate stack in-situ formations. IEICE Electronics Express, 2011, 8, 1492-1497.	0.8	4
31	Ultrathin HfN Multilayer Gate Insulator Formation with High Dielectric Constant Induced by Interface Polarization. , 2019, , .		4
32	Low-Voltage Operation of MFSFET with Ferroelectric Nondoped HfO₂ Formed by Kr/O₂-Plasma Sputtering. , 2020, , .		4
33	MFSFET with 5 nm Thick Ferroelectric Undoped HfO₂ Gate Insulator. , 2021, , .		4
34	Influence of Si(100) surface flattening process on nonvolatile memory characteristics of Hf-based MONOS structures. , 2017, , .		3
35	Reduction of process temperature for Si surface flattening utilizing Ar/H₂ambient annealing and its application to SOI-MISFETs with bilayer HfN high-k gate insulator. Japanese Journal of Applied Physics, 2020, 59, SCCB02.	1.5	3
36	Investigation of the HfON Tunneling Layer of MONOS Device for Low-Voltage and High-Speed Operation Nonvolatile Memory Application. IEEE Transactions on Semiconductor Manufacturing, 2021, 34, 323-327.	1.7	3

#	Article	IF	Citations
37	Effect of ultra-thin Ti layer on PtSi work function modulation. , 2005, , .		2
38	Bias-voltage-dependent measurement of apparent barrier height on low-work-function thin film. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2020, 38, 062801.	1.2	2
39	The Effect of Kr/O₂ Sputtering on the Ferroelectric Properties of SrBi₂Ta₂O₉ Thin Film Formation. IEICE Transactions on Electronics, 2019, E102.C, 441-446.	0.6	2
40	<i>In-Situ</i> N₂-Plasma Nitridation for High-k HfN Gate Insulator Formed by Electron Cyclotron Resonance Plasma Sputtering. IEICE Transactions on Electronics, 2020, E103.C, 299-303.	0.6	2
41	Investigation of random telegraph noise characteristics of Hf-based MONOS nonvolatile memory devices with HfO₂ and HfON tunneling layers. Japanese Journal of Applied Physics, 2022, 61, SC1066.	1.5	2
42	CMOS downsizing and high-K gate insulator technology. , 0, , .		1
43	Effects of gas phase absorption into Si substrates on plasma doping process. , 0, , .		1
44	Multi-level 2-bit/cell operation utilizing Hf-based MONOS nonvolatile memory. , 2018, , .		1
45	Ferroelectric Hafnium Nitride Thin Films Directly Formed on Si(100) Substrate. IEEE Journal of the Electron Devices Society, 2021, 9, 1036-1040.	2.1	1
46	Effects of sputtering power on the formation of 5 nm thick ferroelectric nondoped HfO₂ gate insulator for MFSFET application. Japanese Journal of Applied Physics, 2022, 61, SH1010.	1.5	1
47	A Study on Selective Etching of SiGe Layers in SiGe/Si Systems for Device Applications. Materials Research Society Symposia Proceedings, 2003, 795, 194.	0.1	0
48	Work Function and Electronic Structure Measurements on Nitrogen-Doped LaB6 Thin Film by Scanning Tunneling Microscope. , 2019, , .		0
49	High-k LaBxNy gate insulator formed by the Ar/N2 plasma sputtering of N-doped LaB6 metal thin films and its application to floating-gate memory. , 2020, , .		0
50	The Effect of Si Surface Flattening Process on the MISFET With High-k HfNx Multilayer Gate Dielectrics. IEEE Transactions on Semiconductor Manufacturing, 2021, 34, 328-332.	1.7	0
51	Multi-level 2-bit/cell operation utilizing Hf-based metal/oxide/nitride/oxide/silicon nonvolatile memory with HfO₂ and HfON tunneling layer. Japanese Journal of Applied Physics, 2022, 61, SB1001.	1.5	0