Chong-Min Kyung

List of Publications by Year in Descending Order

59 papers	485 citations	13 h-index	19 g-index
95 ext. papers	627 ext. citations	3.4 avg, IF	3.98 L-index

#	Paper	IF	Citations
59	A Memory- and Accuracy-Aware Gaussian Parameter-Based Stereo Matching Using Confidence Measure. *IEEE Transactions on Pattern Analysis and Machine Intelligence*, **2021**, 43, 1845-1858	13.3	
58	Global Feature Aggregation for Accident Anticipation **2021**,		1
57	Fine-Tuning DARTS for Image Classification **2021**,		4
56	Accurate and Robust Walking Speed Estimation With Adaptive Regression Models for Wrist-Worn Devices. *IEEE Sensors Journal*, **2020**, 20, 10744-10755	4	1
55	Resource-Efficient and High-Throughput VLSI Design of Global Optical Flow Method for Mobile Systems. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 1717-1725	2.6	0
54	Unsupervised deep learning for depth estimation with offset pixels. *Optics Express*, **2020**, 28, 8619-8639	3.3	1
53	On-Chip Depth and Image Sensing System With Offset Pixel Apertures. *IEEE Sensors Journal*, **2020**, 20, 14369-14382	4	
52	Offset Aperture: A Passive Single-Lens Camera for Depth Sensing. *IEEE Transactions on Circuits and Systems for Video Technology*, **2019**, 29, 1380-1393	6.4	4
51	Rejecting Motion Outliers for Efficient Crowd Anomaly Detection. *IEEE Transactions on Information Forensics and Security*, **2019**, 14, 541-556	8	28
50	**2019**,		24
49	Memory-Efficient Parametric Semiglobal Matching. *IEEE Signal Processing Letters*, **2018**, 25, 194-198	3.2	12
48	In-Pixel Aperture CMOS Image Sensor for 2-D and 3-D Imaging. *IEEE Sensors Journal*, **2018**, 18, 9163-9168	4	5
47	A Low-Complexity Pedestrian Detection Framework for Smart Video Surveillance Systems. *IEEE Transactions on Circuits and Systems for Video Technology*, **2017**, 27, 2260-2273	6.4	45
46	Offset aperture based hardware architecture for real-time depth extraction **2017**,		2
45	Memory efficient self guided image filtering **2017**,		2
44	EBSCam: Background Subtraction for Ubiquitous Computing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 1-13	2.6	3
43	Hybrid L2 NUCA Design and Management Considering Data Access Latency, Energy Efficiency, and Storage Lifetime. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3118-3131	2.6	2

42	Design and Implementation of Practical Step Detection Algorithm for Wrist-Worn Devices. *IEEE Sensors Journal*, **2016**, 1-1	4	14
41	Energy-efficient illumination-invariant change detection in DCT coefficient domain for vehicular black box camera. *Electronics Letters*, **2015**, 51, 822-824	1.1	0
40	Runtime Thermal Management for 3-D Chip-Multiprocessors With Hybrid SRAM/MRAM L2 Cache. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 520-533	2.6	8
39	Hardware architecture and optimization of sliding window based pedestrian detection on FPGA for high resolution images by varying local features **2015**,		4
38	A solar energy harvesting system for a portable compact LED lamp **2015**,		3
37	Static energy minimization of 3D stacked L2 cache with selective cache compression **2013**,		3
36	Energy-Aware Video Encoding for Image Quality Improvement in Battery-Operated Surveillance Camera. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2012**, 20, 310-318	2.6	18
35	Hybrid cache architecture replacing SRAM cache with future memory technology **2012**,		7
34	Thermal-aware energy minimization of 3D-stacked L3 cache with error rate limitation **2011**,		7
33	Runtime Power Management of 3-D Multi-Core Architectures Under Peak Power and Temperature Constraints. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2011**, 30, 905-918	2.5	24
32	Maximizing throughput of temperature-constrained multi-core systems with 3D-stacked cache memory **2011**,		4
31	Energy minimization of 3D cache-stacked processor based on thin-film thermoelectric coolers **2011**,		2
30	A Dynamic Search Range Algorithm for Stabilized Reduction of Memory Traffic in Video Encoder. *IEEE Transactions on Circuits and Systems for Video Technology*, **2010**, 20, 1041-1046	6.4	5
29	Performance maximization of 3D-stacked cache memory on DVFS-enabled processor **2010**,		1
28	Temperature-Aware Integrated DVFS and Power Gating for Executing Tasks With Runtime Distribution. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 1381-1394	2.5	16
27	Topology Synthesis for Low Power Cascaded Crossbar Switches. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2010**, 29, 2041-2045	2.5	5
26	Design of energy-aware video codec-based system **2010**,		3
25	A Lossless Embedded Compression Using Significant Bit Truncation for HD Video Coding. *IEEE Transactions on Circuits and Systems for Video Technology*, **2010**, 20, 848-860	6.4	50

24	Dynamic-Range Widening in a CMOS Image Sensor Through Exposure Control Over a Dual-Photodiode Pixel. *IEEE Transactions on Electron Devices*, **2009**, 56, 3000-3008	2.9	8
23	A lossless embedded compression algorithm for high definition video coding **2009**,		9
22	Selective Search Area Reuse Algorithm for Low External Memory Access Motion Estimation. *IEEE Transactions on Circuits and Systems for Video Technology*, **2009**, 19, 1044-1050	6.4	13
21	A Multi-layer motion estimation scheme for spatial scalability in H.264/AVC scalable extension **2009** ,		5
20	Lossless frame memory recompression for video codec preserving random accessibility of coding unit. *IEEE Transactions on Consumer Electronics*, **2009**, 55, 2105-2113	4.8	16
19	Power Minimization for Dual- and Triple-Supply Digital Circuits via Integer Linear Programming. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2009**, E92-A, 2318-2325	0.4	
18	Suppressing rolling-shutter distortion of CMOS image sensors by motion vector detection. *IEEE Transactions on Consumer Electronics*, **2008**, 54, 1479-1487	4.8	25
17	Task partitioning algorithm for intra-task dynamic voltage scaling **2008**,		1
16	Performance-driven event-based synchronization for multi-FPGA simulation accelerator with event time-multiplexing bus. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2005**, 24, 1444-1456	2.5	4
15	ATOMi: an algorithm for circuit partitioning into multiple FPGAs using time-multiplexed, off-chip, multicasting interconnection architecture. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2005**, 13, 861-864	2.6	1
14	CONSCEP: A CONFIGURABLE SoC EMULATION PLATFORM FOR C-BASED FAST PROTOTYPING. *Journal of Circuits, Systems and Computers*, **2005**, 14, 137-157	0.9	
13	CeRA: a router for symmetrical FPGAs based on exact routing density evaluation. *IEEE Transactions on Computers*, **2004**, 53, 829-842	2.5	1
12	Exploiting intellectual properties with imprecise design costs for system-on-chip synthesis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 240-252	2.6	4
11	Conforming block inversion for low power memory. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2002**, 10, 15-19	2.6	3
10	MetaCore: an application-specific programmable DSP development system. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2000**, 8, 173-183	2.6	6
9	DIVA: dual-issue VLIW architecture with media instructions for image processing. *IEEE Transactions on Consumer Electronics*, **1999**, 45, 192-202	4.8	
8	Synthesis of application specific instructions for embedded DSP software. *IEEE Transactions on Computers*, **1999**, 48, 603-614	2.5	38
7	MDSP-II: a 16-bit DSP with mobile communication accelerator. *IEEE Journal of Solid-State Circuits*, **1999**, 34, 397-404	5.5	8

6	Design Verification of Complex Microprocessors. *Journal of Circuits, Systems and Computers*, **1997**, 07, 301-318	0.9	0
5	A new parallel ray-tracing system based on object decomposition. *Visual Computer*, **1996**, 12, 244-253	2.3	5
4	Verification methodology of compatible microprocessors		1
3	A hardware accelerator for the specular intensity of Phong illumination model in 3-dimensional graphics		1
2	Exploiting intellectual properties in ASIP designs for embedded DSP software		3
1	Reducing cross-coupling among interconnect wires in deep-submicron datapath design		22