Chong-Min Kyung

List of Publications by Year
in descending order

95	793	758635 12	642321 23
papers	citations	h-index	g-index

95	95	95	624
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A Lossless Embedded Compression Using Significant Bit Truncation for HD Video Coding. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 848-860.	5.6	76
2	A Low-Complexity Pedestrian Detection Framework for Smart Video Surveillance Systems. IEEE Transactions on Circuits and Systems for Video Technology, 2017, 27, 2260-2273.	5.6	64
3	Rejecting Motion Outliers for Efficient Crowd Anomaly Detection. IEEE Transactions on Information Forensics and Security, 2019, 14, 541-556.	4.5	58
4	Efficient Neural Network Compression. , 2019, , .		54
5	Synthesis of application specific instructions for embedded DSP software. IEEE Transactions on Computers, 1999, 48, 603-614.	2.4	52
6	Suppressing rolling-shutter distortion of CMOS image sensors by motion vector detection. IEEE Transactions on Consumer Electronics, 2008, 54, 1479-1487.	3.0	35
7	Runtime Power Management of 3-D Multi-Core Architectures Under Peak Power and Temperature Constraints. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 905-918.	1.9	31
8	Energy-Aware Video Encoding for Image Quality Improvement in Battery-Operated Surveillance Camera. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 310-318.	2.1	25
9	Reducing cross-coupling among interconnect wires in deep-submicron datapath design. , 0, , .		24
10	Lossless frame memory recompression for video codec preserving random accessibility of coding unit. IEEE Transactions on Consumer Electronics, 2009, 55, 2105-2113.	3.0	23
11	Design and Implementation of Practical Step Detection Algorithm for Wrist-worn Devices. IEEE Sensors Journal, 2016, , 1-1.	2.4	23
12	A lossless embedded compression algorithm for high definition video coding. , 2009, , .		22
13	Temperature-Aware Integrated DVFS and Power Gating for Executing Tasks With Runtime Distribution. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1381-1394.	1.9	21
14	Selective Search Area Reuse Algorithm for Low External Memory Access Motion Estimation. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1044-1050.	5.6	18
15	MetaCore: an application-specific programmable DSP development system. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2000, 8, 173-183.	2.1	17
16	Memory-Efficient Parametric Semiglobal Matching. IEEE Signal Processing Letters, 2018, 25, 194-198.	2.1	16
17	Fine-Tuning DARTS for Image Classification. , 2021, , .		15
18	MDSP-II: a 16-bit DSP with mobile communication accelerator. IEEE Journal of Solid-State Circuits, 1999, 34, 397-404.	3.5	13

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19	Performance-driven event-based synchronization for multi-FPGA simulation accelerator with event time-multiplexing bus. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2005, 24, 1444-1456.	1.9	11
20	Runtime Thermal Management for 3-D Chip-Multiprocessors With Hybrid SRAM/MRAM L2 Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 520-533.	2.1	10
21	Dynamic-Range Widening in a CMOS Image Sensor Through Exposure Control Over a Dual-Photodiode Pixel. IEEE Transactions on Electron Devices, 2009, 56, 3000-3008.	1.6	9
22	Thermal-aware energy minimization of 3D-stacked L3 cache with error rate limitation. , 2011, , .		9
23	Hybrid cache architecture replacing SRAM cache with future memory technology. , 2012, , .		9
24	A new parallel ray-tracing system based on object decomposition. Visual Computer, 1996, 12, 244-253.	2.5	8
25	Hardware architecture and optimization of sliding window based pedestrian detection on FPGA for high resolution images by varying local features. , 2015, , .		8
26	A Multi-layer motion estimation scheme for spatial scalability in H.264/AVC scalable extension. , 2009, , .		7
27	In-Pixel Aperture CMOS Image Sensor for 2-D and 3-D Imaging. IEEE Sensors Journal, 2018, 18, 9163-9168.	2.4	7
28	Exploiting intellectual properties with imprecise design costs for system-on-chip synthesis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 240-252.	2.1	6
29	A Dynamic Search Range Algorithm for Stabilized Reduction of Memory Traffic in Video Encoder. IEEE Transactions on Circuits and Systems for Video Technology, 2010, 20, 1041-1046.	5.6	6
30	Topology Synthesis for Low Power Cascaded Crossbar Switches. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 2041-2045.	1.9	6
31	Maximizing throughput of temperature-constrained multi-core systems with 3D-stacked cache memory. , 2011, , .		6
32	A solar energy harvesting system for a portable compact LED lamp. , 2015, , .		6
33	Offset Aperture: A Passive Single-Lens Camera for Depth Sensing. IEEE Transactions on Circuits and Systems for Video Technology, 2019, 29, 1380-1393.	5.6	6
34	Global Feature Aggregation for Accident Anticipation. , 2021, , .		6
35	Verification methodology of compatible microprocessors. , 0, , .		5
36	Automatic translation of behavioral testbench for fully accelerated simulation. , 0, , .		5

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37	Accurate and Robust Walking Speed Estimation With Adaptive Regression Models for Wrist-Worn Devices. IEEE Sensors Journal, 2020, 20, 10744-10755.	2.4	5
38	Resource-Efficient and High-Throughput VLSI Design of Global Optical Flow Method for Mobile Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1717-1725.	2.1	5
39	Hybrid L2 NUCA Design and Management Considering Data Access Latency, Energy Efficiency, and Storage Lifetime. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 3118-3131.	2.1	4
40	Exploiting intellectual properties in ASIP designs for embedded DSP software. , 0, , .		3
41	Pyramid texture compression and decompression using interpolative vector quantization. , 2000, , .		3
42	Conforming block inversion for low power memory. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2002, 10, 15-19.	2.1	3
43	ATOMi: an algorithm for circuit partitioning into multiple FPGAs using time-multiplexed, off-chip, multicasting interconnection architecture. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 861-864.	2.1	3
44	Task partitioning algorithm for intra-task dynamic voltage scaling. , 2008, , .		3
45	Design of energy-aware video codec-based system. , 2010, , .		3
46	Static energy minimization of 3D stacked L2 cache with selective cache compression. , 2013, , .		3
47	EBSCam: Background Subtraction for Ubiquitous Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-13.	2.1	3
48	Design Verification of Complex Microprocessors. Journal of Circuits, Systems and Computers, 1997, 07, 301-318.	1.0	2
49	A C-based RTL Design Verification Methodology For Complex Microprocessor. , 0, , .		2
50	MetaCore: a configurable & instruction-level extensible DSP core. , 0, , .		2
51	A hardware accelerator for the specular intensity of Phong illumination model in 3-dimensional graphics. , 0, , .		2
52	SoC Design Environment with Automated Configurable Bus Generation for Rapid Prototyping. , 0, , .		2
53	Performance maximization of 3D-stacked cache memory on DVFS-enabled processor. , 2010, , .		2
54	Energy minimization of 3D cache-stacked processor based on thin-film thermoelectric coolers. , 2011, , .		2

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55	Squeezing maximizing performance out of 3D cache-stacked multicore architectures. , 2011, , .		2
56	A low error add and shift-based efficient implementation of base-2 logarithm. , 2017, , .		2
57	Offset aperture based hardware architecture for real-time depth extraction. , 2017, , .		2
58	Memory efficient self guided image filtering. , 2017, , .		2
59	Design verification of complex microprocessors. , 0, , .		1
60	CBLO: a clustering based linear ordering for netlist partitioning. , 0, , .		1
61	Multiple behavior module synthesis based on selective groupings. , 0, , .		1
62	Virtual chip: making functional models work on real target systems. , 0, , .		1
63	A multi-threading MPEG processor with variable issue modes. , 0, , .		1
64	CeRA: a router for symmetrical FPGAs based on exact routing density evaluation. IEEE Transactions on Computers, 2004, 53, 829-842.	2.4	1
65	A fast CABAC rate estimator for H.264/AVC mode decision. , 2009, , .		1
66	Temperature- and bus traffic- aware data placement in 3D-stacked cache. , 2010, , .		1
67	Latency-aware Utility-based NUCA Cache Partitioning in 3D-stacked multi-processor systems. , 2010, , .		1
68	An energy-aware hierarchical event detection in battery-operated wireless video surveillance systems. , 2011, , .		1
69	Development of hematocrit monitoring sensor using screen printed carbon electrode. , 2013, , .		1
70	Energyâ€efficient illuminationâ€invariant change detection in DCT coefficient domain for vehicular black box camera. Electronics Letters, 2015, 51, 822-824.	0.5	1
71	Memory efficient hardware accelerator for kernel support vector machine based pedestrian detection. , 2016, , .		1
72	Practical Inter-Floor Noise Sensing System with Localization and Classification. Sensors, 2019, 19, 3633.	2.1	1

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73	A Memory- and Accuracy-Aware Gaussian Parameter-Based Stereo Matching Using Confidence Measure. IEEE Transactions on Pattern Analysis and Machine Intelligence, 2021, 43, 1845-1858.	9.7	1
74	Unsupervised deep learning for depth estimation with offset pixels. Optics Express, 2020, 28, 8619.	1.7	1
75	MetaCore: an application specific DSP development system. , 0, , .		0
76	Single cycle access cache for the misaligned data and instruction prefetch. , 0, , .		0
77	Architecture selection of a flexible DSP core using reconfigurable system software. , 0, , .		0
78	A floorplan-based planning methodology for power and clock distribution in ASICs [CMOS technology]. , 0, , .		0
79	DIVA: dual-issue VLIW architecture with media instructions for image processing. IEEE Transactions on Consumer Electronics, 1999, 45, 192-202.	3.0	0
80	Node sampling technique to speed up probability-based power estimation methods. , 1999, , .		0
81	3D geometry graphics system using deferred primitive rendering with VLIW geometry processor. , 0, , .		0
82	Fast development of source-level debugging system using hardware emulation. , 0, , .		0
83	iSAVE: a behavioral emulator for in-system algorithm verification. , 0, , .		0
84	3D graphics system with VLIW processor for geometry acceleration. , 0, , .		0
85	CONSCEP: A CONFIGURABLE SoC EMULATION PLATFORM FOR C-BASED FAST PROTOTYPING. Journal of Circuits, Systems and Computers, 2005, 14, 137-157.	1.0	0
86	Multimedia application extension processor(MAEP). , 2008, , .		0
87	Data Reuse method between Heterogeneous Partitions (DRHP) in H.264/AVC motion compensator. , 2008, , .		0
88	Power Minimization for Dual- and Triple-Supply Digital Circuits via Integer Linear Programming. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 2318-2325.	0.2	0
89	Exploiting maximum throughput in 3D multicore architectures with stacked NUCA cache. , 2011, , .		0
90	Integration of cache data allocation and voltage/frequency scaling for temperature-constrained multi-core systems with 3-D stacked cache memory. , 2011, , .		0

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91	Cost-effective TSV redundancy configuration. , 2012, , .		0
92	Energy-efficient and fast collection method for smart sensor monitoring systems. , 2013, , .		0
93	Real-time depth map processor for offset aperture based single camera system. , 2018, , .		0
94	On-Chip Depth and Image Sensing System With Offset Pixel Apertures. IEEE Sensors Journal, 2020, 20, 14369-14382.	2.4	0
95	Synthesis of application specific instructions for embedded DSP software. , 0, , .		0