Yung-Chih Chen

List of Publications by Year
in descending order

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60	253	1163117 8	1281871 11
papers	citations	h-index	g-index

60	60	60	105
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Donâ€™t Care Computation and De Morgan Transformation for Threshold Logic Network Optimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1412-1422.	2.7	0
2	Majority Logic Circuit Minimization Using Node Addition and Removal. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 642-655.	2.7	2
3	LOOPLock 2.0: An Enhanced Cyclic Logic Locking Approach. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 29-34.	2.7	8
4	An Efficient Approximate Node Merging with an Error Rate Guarantee. , 2021, , .		2
5	Dynamic Workload Allocation for Edge Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 519-529.	3.1	8
6	On Synthesizing Memristor-Based Logic Circuits in Area-Constrained Crossbar Arrays. , 2021, , .		0
7	Diagnosis for Reconfigurable Single-Electron Transistor Arrays with a More Generalized Defect Model. ACM Journal on Emerging Technologies in Computing Systems, 2021, 17, 1-23.	2.3	0
8	1st-Order to 2nd-Order Threshold Logic Gate Transformation with an Enhanced ILP-based Identification Method. , 2021, , .		0
9	On Reduction of Computations for Threshold Function Identification. , 2021, , .		0
10	LOOPLock: Logic Optimization-Based Cyclic Logic Locking. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2178-2191.	2.7	11
11	Accuracy Tolerant Neural Networks Under Aggressive Power Optimization. , 2020, , .		1
12	SMARTLock: SAT Attack and Removal Attack-Resistant Tree-Based Logic Locking. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2020, E103.A, 733-740.	0.3	1
13	A New Necessary Condition for Threshold Function Identification. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 5304-5308.	2.7	5
14	A Convolutional Result Sharing Approach for Binarized Neural Network Inference. , 2020, , .		3
15	Donâ€™t-Care-Based Node Minimization for Threshold Logic Networks. , 2020, , .		0
16	Threshold Function Identification by Redundancy Removal and Comprehensive Weight Assignments. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 2284-2297.	2.7	8
17	A Glitch Key-Gate for Logic Locking. , 2019, , .		0
18	A Smart Single-Sensor Device for Instantaneously Monitoring Lower Limb Exercises. , 2019, , .		4

#	Article	IF	Citations
19	Optimization of Threshold Logic Networks with Node Merging and Wire Replacement. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-18.	2.6	8
20	On Synthesizing Memristor-Based Logic Circuits With Minimal Operational Pulses. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2842-2852.	3.1	22
21	Logic optimization with considering boolean relations. , 2018, , .		1
22	Efficient synthesis of approximate threshold logic circuits with an error rate guarantee. , 2018, , .		4
23	Optimization of threshold logic networks with ODC-based node merging. , 2018, , .		2
24	Using range-equivalent circuits for facilitating bounded sequential equivalence checking. , 2018, , .		0
25	Contactless Testing for Prebond Interposers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1005-1014.	3.1	0
26	Dynamic Diagnosis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 1477-1489.	3.1	2
27	Majority logic circuits optimisation by node merging. , 2017, , .		8
28	In&Out: Restructuring for threshold logic network optimization. , 2017, , .		5
29	Tree-Based Logic Encryption for Resisting SAT Attack. , 2017, , .		4
30	A counterexample-based debugging method for reconfigurable single-electron transistor arrays. , 2017, , .		0
31	Minimization of Number of Neurons in Voronoi Diagram-Based Artificial Neural Networks. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 225-233.	2.4	3
32	MajorSat: A SAT solver to majority logic. , 2016, , .		2
33	Fast synthesis of threshold logic networks with optimization. , 2016, , .		12
34	Diagnosis and Synthesis for Defective Reconfigurable Single-Electron Transistor Arrays. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, , 1-14.	3.1	3
35	Using Structural Relations for Checking Combinationality of Cyclic Circuits. , 2015, , .		0
36	Synthesis and verification of cyclic combinational circuits. , 2015, , .		5

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37	Correctness Analysis and Power Optimization for Probabilistic Boolean Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 615-628.	2.7	2
38	A defect-aware approach for mapping reconfigurable Single-Electron Transistor arrays. , 2015, , .		4
39	Synthesis for Width Minimization in the Single-Electron Transistor Array. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2862-2875.	3.1	5
40	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2
41	Rewiring for threshold logic circuit minimization. , 2014, , .		0
42	SAT-based complete logic implication with application to logic optimization. , 2014, , .		0
43	Width minimization in the Single-Electron Transistor array synthesis. , 2014, , .		2
44	Rewiring for threshold logic circuit minimization. , 2014, , .		1
45	Sensitization criterion for threshold logic circuits and its application. , 2013, , .		4
46	Verification of Reconfigurable Binary Decision Diagram-Based Single-Electron Transistor Arrays. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2013, 32, 1473-1483.	2.7	10
47	On Reconfigurable Single-Electron Transistor Arrays Synthesis Using Reordering Techniques. , 2013, , .		12
48	A probabilistic analysis method for functional qualification under Mutation Analysis. , 2012, , .		1
49	Logic Restructuring Using Node Addition and Removal. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 260-270.	2.7	11
50	Fast Node Merging With Don't Cares Using Logic Implications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1827-1832.	2.7	22
51	A novel ACO-based pattern generation for peak power estimation in VLSI circuits. , 2009, , .		3
52	An efficient approach to sip design integration. , 2009, , .		3
53	Dependent-Latch Identification in Reachable State Space. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 1113-1126.	2.7	1
54	Fast detection of node mergers using logic implications. , 2009, , .		24

#	ARTICLE	IF	CITATIONS
55	An Implicit Approach to Minimizing Range-Equivalent Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1942-1955.	2.7	3
56	Novel Probabilistic Combinational Equivalence Checking. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 365-375.	3.1	4
57	Multiple error diagnosis in large combinational circuits using an efficient parallel vector simulation. , 2008, , .		0
58	A Statistic-Based Approach to Testability Analysis. , 2008, , .		2
59	An improved approach for alternative wires identification. , 0, , .		3
60	Language-Based High Level Transaction Extraction on On-chip Buses. , 0, , .		0