Sanghamitra Roy

List of Publications by Year
in descending order

61	495	1307594 7	1199594 12
papers	citations	h-index	g-index

61	61	61	368
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Probabilistic Verification for Reliability of a Two-by-Two Network-on-Chip System. Lecture Notes in Computer Science, 2021, , 232-248.	1.3	2
2	Understanding Security Threats in Emerging Neuromorphic Computing Architecture. Journal of Hardware and Systems Security, 2021, 5, 45-57.	1.3	2
3	EFFORT: A Comprehensive Technique to Tackle Timing Violations and Improve Energy Efficiency of Near-Threshold Tensor Processing Units. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021, 29, 1790-1799.	3.1	5
4	UPTPU: Improving Energy Efficiency of a Tensor Processing Unit through Underutilization Based Power-Gating. , 2021, , .		2
5	Exploring Warp Criticality in Near-Threshold GPGPU Applications Using a Dynamic Choke Point Analysis. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 456-466.	3.1	1
6	Challenges and Opportunities in Near-Threshold DNN Accelerators around Timing Errors. Journal of Low Power Electronics and Applications, 2020, 10, 33.	2.0	5
7	GreenTPU: Predictive Design Paradigm for Improving Timing Error Resilience of a Near-Threshold Tensor Processing Unit. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1557-1566.	3.1	11
8	EFFORT: Enhancing Energy Efficiency and Error Resilience of a Near-Threshold Tensor Processing Unit. , 2020, , .		10
9	GreenTPU. , 2019, , .		25
10	Energy Efficient Network-on-Chip Architectures for Many-Core Near-Threshold Computing System. Journal of Low Power Electronics, 2019, 15, 115-128.	0.6	1
11	Securing Data Center Against Power Attacks. Journal of Hardware and Systems Security, 2019, 3, 177-188.	1.3	4
12	Probabilistic Verification for Reliable Network-on-Chip System Design. Lecture Notes in Computer Science, 2019, , 110-126.	1.3	2
13	TITAN: Uncovering the Paradigm Shift in Security Vulnerability at Near-Threshold Computing. IEEE Transactions on Emerging Topics in Computing, 2018, , 1-1.	4.6	2
14	FIFA: Exploring a Focally Induced Fault Attack Strategy in Near-Threshold Computing. IEEE Embedded Systems Letters, 2018, 10, 115-118.	1.9	0
15	Dynamic Choke Sensing for Timing Error Resilience in NTC Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1-10.	3.1	7
16	TASPDetect: Reviving Trust in 3PIP By Detecting TASP Trojans. Microprocessors and Microsystems, 2018, 56, 76-83.	2.8	1
17	ACE-GPU. , 2018, , .		5
18	Trident: A comprehensive timing error resilient technique against choke points at NTC. , 2018, , .		0

#	Article	IF	Citations
19	Trident: Comprehensive Choke Error Mitigation in NTC Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2195-2204.	3.1	2
20	SSAGA. ACM Transactions on Design Automation of Electronic Systems, 2017, 22, 1-20.	2.6	1
21	Security Measures Against a Rogue Network-on-Chip. Journal of Hardware and Systems Security, 2017, 1, 173-187.	1.3	7
22	Revamping timing error resilience to tackle choke points at NTC systems. , 2017, , .		7
23	IcoNoClast: Tackling Voltage Noise in the NoC Power Supply Through Flow-Control and Routing Algorithms. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 2035-2044.	3.1	5
24	SwiftGPU. , 2016, , .		7
25	PRADA: Combating Voltage Noise in the NoC Power Supply Through Flow-Control and Routing Algorithms. , 2016, , .		1
26	DARP-MP. ACM Transactions on Design Automation of Electronic Systems, 2015, 21, 1-21.	2.6	2
27	Runtime Detection of a Bandwidth Denial Attack from a Rogue Network-on-Chip. , 2015, , .		22
28	Wearout Resilience in NoCs Through an Aging Aware Adaptive Routing Algorithm. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 369-373.	3.1	11
29	Resilient Cache Design for Mobile Processors in the Near-Threshold Regime. Journal of Low Power Electronics, 2015, 11, 112-120.	0.6	1
30	Fort-NoCs. , 2014, , .		86
31	Tackling QoS-induced aging in exascale systems through agile path selection. , 2014, , .		2
32	Dark Silicon Aware Multicore Systems: Employing Design Automation With Architectural Insight. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 1192-1196.	3.1	10
33	Exploring High-Throughput Computing Paradigm for Global Routing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 155-167.	3.1	15
34	Exploiting static and dynamic locality of timing errors in robust L1 cache design. , 2014, , .		1
35	Long term sustainability of differentially reliable systems in the dark silicon era. , 2013, , .		2
36	A global router on GPU architecture. , 2013, , .		9

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37	Proactive Aging Management in Heterogeneous NoCs through a Criticality-driven Routing Approach. , 2013, , .		16
38	Architecturally Homogeneous Power-Performance Heterogeneous Multicore Systems. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 670-679.	3.1	8
39	Efficiently tolerating timing violations in pipelined microprocessors. , 2013, , .		12
40	Maximising energy efficiency in 3D multicore systems: a formalised approach. International Journal of Electronics, 2013, 100, 150-170.	1.4	1
41	Using Adaptive Body Biasing for Robust Process Variation Aware DRAM Design. Journal of Low Power Electronics, 2013, 9, 23-36.	0.6	0
42	Towards graceful aging degradation in NoCs through an adaptive routing algorithm. , 2012, , .		27
43	Process variation aware DRAM design using block based adaptive body biasing algorithm. , 2012, , .		3
44	An MILP-based aging-aware routing algorithm for NoCs. , 2012, , .		13
45	DOC: Fast and accurate congestion analysis for global routing. , 2012, , .		1
46	Mitigating NBTI in the physical register file through stress prediction. , 2012, , .		5
47	Power-Performance Yield optimization for MPSoCs using MILP. , 2012, , .		7
48	Analysis of intermittent timing fault vulnerability. Microelectronics Reliability, 2012, 52, 1515-1522.	1.7	7
49	Predicting timing violations through instruction-level path sensitization analysis. , 2012, , .		19
50	Exploring high throughput computing paradigm for global routing. , 2011, , .		5
51	Integrated circuit-architectural framework for PSN aware floorplanning in microprocessors. , 2011, , .		2
52	Optimizing simulated annealing on GPU: A case study with IC floorplanning. , 2011, , .		11
53	Analysis and mitigation of NBTI aging in register file: An end-to-end approach. , 2011, , .		18
54	A GPU Algorithm for IC Floorplanning: Specification, Analysis and Optimization. , 2011, , .		1

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55	Microprocessor Power Supply Noise Aware Floorplanning Using a Circuit-Architectural Framework. Journal of Low Power Electronics, 2011, 7, 303-313.	0.6	0
56	A convex optimization framework for leakage aware thermal provisioning in 3D multicore architectures. , 2010, , .		1
57	Microarchitecture aware gate sizing: A framework for circuit-architecture co-optimization. , 2010, , .		2
58	Rethinking Threshold Voltage Assignment in 3D Multicore Designs. , 2010, , .		11
59	A Novel Threshold Voltage Assignment for 3D Multicore Designs. Journal of Low Power Electronics, 2010, 6, 436-446.	0.6	1
60	An Algorithm for Trading Off Quantization Error with Hardware Resources for MATLAB-Based FPGA Design. IEEE Transactions on Computers, 2005, 54, 886-896.	3.4	40
61	Convexfit: an optimal minimum-error convex fitting and smoothing algorithm with application to gate-sizing. , 0, , .		8