Cheng, Tim Kwang-Ting

List of Publications by Year in Descending Order

164 papers	3,092 citations	27 h-index	49 g-index
197 ext. papers	4,122 ext. citations	5 avg, IF	5.5 L-index

#	Paper	IF	Citations
164	Adaptive Contrast for Image Regression in Computer-Aided Disease Assessment.. *IEEE Transactions on Medical Imaging*, **2021**, PP,	11.7	1
163	HyCA: A Hybrid Computing Architecture for Fault Tolerant Deep Learning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 1-1	2.5	1
162	Variation-Aware Federated Learning With Multi-Source Decentralized Medical Image Data. *IEEE Journal of Biomedical and Health Informatics*, **2021**, 25, 2615-2628	7.2	10
161	Roadmap on emerging hardware and technology for machine learning. *Nanotechnology*, **2021**, 32, 012002	3.4	45
160	Energy Efficiency and Yield Optimization for Optical Interconnects via Transceiver Grouping. *Journal of Lightwave Technology*, **2021**, 39, 1567-1578	4	1
159	Fast Depth Prediction and Obstacle Avoidance on a Monocular Drone Using Probabilistic Convolutional Neural Network. *IEEE Transactions on Intelligent Transportation Systems*, **2021**, 22, 156-167	6.1	11
158	R2F: A Remote Retraining Framework for AIoT Processors With Computing Errors. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 1-12	2.6	0
157	Ratio-based multi-level resistive memory cells. *Scientific Reports*, **2021**, 11, 1351	4.9	3
156	Reliability Evaluation and Analysis of FPGA-Based Neural Network Acceleration System. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 472-484	2.6	10
155	Joint Multi-Dimension Pruning via Numerical Gradient Update. *IEEE Transactions on Image Processing*, **2021**, 30, 8034-8045	8.7	1
154	Multi-Task Siamese Network for Retinal Artery/Vein Separation via Deep Convolution Along Vessel. *IEEE Transactions on Medical Imaging*, **2020**, 39, 2904-2919	11.7	8
153	Process design kit and design automation for flexible hybrid electronics. *Journal of the Society for Information Display*, **2020**, 28, 241-251	2.1	0
152	Enabling a Single Deep Learning Model for Accurate Gland Instance Segmentation: A Shape-Aware Adversarial Learning Framework. *IEEE Transactions on Medical Imaging*, **2020**, 39, 2176-2189	11.7	11
151	Imitation Learning-based Algorithm for Drone Cinematography System. *IEEE Transactions on Cognitive and Developmental Systems*, **2020**, 1-1	3	
150	Characterization and Applications of Spatial Variation Models for Silicon Microring-Based Optical Transceivers **2020**,		2
149	Persistent Fault Analysis of Neural Networks on FPGA-based Acceleration System **2020**,		4
148	Robust Design of Large Area Flexible Electronics via Compressed Sensing **2020**,		2

147	Semi-supervised mp-MRI data synthesis with StitchLayer and auxiliary distance maximization. *Medical Image Analysis*, **2020**, 59, 101565	15.4	11
146	Bi-Real Net: Binarizing Deep Network Towards Real-Network Performance. *International Journal of Computer Vision*, **2020**, 128, 202-219	10.6	15
145	Bi-Modality Medical Image Synthesis Using Semi-Supervised Sequential Generative Adversarial Networks. *IEEE Journal of Biomedical and Health Informatics*, **2020**, 24, 855-865	7.2	10
144	16-4: Invited Paper: Process Design Kit and Design Automation for Flexible Hybrid Electronics. *Digest of Technical Papers SID International Symposium*, **2019**, 50, 217-220	0.5	1
143	Ultra-thin Skin Electronics for High Quality and Continuous Skin-Sensor-Silicon Interfacing **2019**,		2
142	Low-voltage high-performance flexible digital and analog circuits based on ultrahigh-purity semiconducting carbon nanotubes. *Nature Communications*, **2019**, 10, 2161	17.4	80
141	. *IEEE Transactions on Multimedia*, **2019**, 21, 2701-2713	6.6	14
140	Bidirectional tuning of microring-based silicon photonic transceivers for optimal energy efficiency **2019**,		3
139	. *IEEE Transactions on Multimedia*, **2019**, 21, 470-483	6.6	22
138	Real-Time Semantic Plane Reconstruction on a Monocular Drone Using Sparse Fusion. *IEEE Transactions on Vehicular Technology*, **2019**, 68, 7383-7391	6.8	6
137	Taming Emerging DevicesUVariation and Reliability Challenges with Architectural and System Solutions [Invited] **2019**,		2
136	Compact Modeling of Thin-Film Transistors for Flexible Hybrid IoT Design. *IEEE Design and Test*, **2019**, 36, 6-14	1.4	8
135	MetaPruning: Meta Learning for Automatic Neural Network Channel Pruning **2019**,		112
134	A Three-Stage Deep Learning Model for Accurate Retinal Vessel Segmentation. *IEEE Journal of Biomedical and Health Informatics*, **2019**, 23, 1427-1436	7.2	114
133	Process design kit for flexible hybrid electronics **2018**,		12
132	Joint Segment-Level and Pixel-Wise Losses for Deep Learning Based Retinal Vessel Segmentation. *IEEE Transactions on Biomedical Engineering*, **2018**, 65, 1912-1923	5	177
131	Automated Detection of Clinically Significant Prostate Cancer in mp-MRI Images Based on an End-to-End Deep Neural Network. *IEEE Transactions on Medical Imaging*, **2018**, 37, 1127-1139	11.7	64
130	Compact modeling of carbon nanotube thin film transistors for flexible circuit design **2018**,		7

129	Robust and real-time pose tracking for augmented reality on mobile devices. *Multimedia Tools and Applications*, **2018**, 77, 6607-6628	2.5	9
128	Resistive random-access memory based on ratioed memristors. *Nature Electronics*, **2018**, 1, 466-472	28.4	40
127	A Skeletal Similarity Metric for Quality Evaluation of Retinal Vessel Segmentation. *IEEE Transactions on Medical Imaging*, **2018**, 37, 1045-1057	11.7	23
126	Energy-efficient channel alignment of DWDM silicon photonic transceivers **2018**,		2
125	A lightweight piecewise linear synthesis method for standard 12-lead ECG signals based on adaptive region segmentation. *PLoS ONE*, **2018**, 13, e0206170	3.7	5
124	ACT: An Autonomous Drone Cinematography System for Action Scenes **2018**,		21
123	Monocular Camera Based Real-Time Dense Mapping Using Generative Adversarial Network **2018**,		6
122	Pairing of microring-based silicon photonic transceivers for tuning power optimization **2018**,		4
121	Accurate face alignment and adaptive patch selection for heart rate estimation from videos under realistic scenarios. *PLoS ONE*, **2018**, 13, e0197275	3.7	6
120	An artificial neural network approach for screening test escapes **2017**,		1
119	3D-DPE: A 3D high-bandwidth dot-product engine for high-performance neuromorphic computing **2017**,		5
118	Biocompatible and totally disintegrable semiconducting polymer for ultrathin and ultralightweight transient electronics. *Proceedings of the National Academy of Sciences of the United States of America*, **2017**, 114, 5107-5112	11.5	255
117	An automated method for accurate vessel segmentation. *Physics in Medicine and Biology*, **2017**, 62, 3757-3778	3.8	13
116	Co-trained convolutional neural networks for automated detection of prostate cancer in multi-parametric MRI. *Medical Image Analysis*, **2017**, 42, 212-227	15.4	73
115	Robust design and design automation for flexible hybrid electronics **2017**,		10
114	Process-variation tolerant flexible circuit for wearable electronics **2016**,		2
113	Spatial pattern analysis of process variations in silicon microring modulators **2016**,		1
112	In-place Repair for Resistive Memories Utilizing Complementary Resistive Switches **2016**,		1

111	Associative Memristive Memory for Approximate Computing in GPUs. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2016**, 6, 222-234	5.2	16
110	A low-power hybrid reconfigurable architecture for resistive random-access memories **2016**,		5
109	Toward large-scale access-transistor-free memristive crossbars **2015**,		11
108	A configurable CMOS memory platform for 3D-integrated memristors **2015**,		8
107	Vertical integration of memristors onto foundry CMOS dies using wafer-scale integration **2015**,		6
106	Architecting energy efficient crossbar-based memristive random-access memories **2015**,		11
105	Standard 12-lead ECG synthesis using a GA optimized BP neural network **2015**,		3
104	Variation-aware adaptive tuning for nanophotonic interconnects **2015**,		10
103	HReRAM: A hybrid reconfigurable resistive random-access memory **2015**,		7
102	Compact modeling and system implications of microring modulators in nanophotonic interconnects **2015**,		8
101	Joint Virtual Probe: Joint exploration of multiple test items' spatial patterns for efficient silicon characterization and test prediction **2014**,		6
100	Test-Quality Optimization for Variable n -Detections of Transition Faults. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 1738-1749	2.6	14
99	Learning from Production Test Data: Correlation Exploration and Feature Engineering **2014**,		7
98	Real-time lossless ECG compression for low-power wearable medical devices based on adaptive region prediction. *Electronics Letters*, **2014**, 50, 1904-1906	1.1	29
97	Feature engineering with canonical analysis for effective statistical tests screening test escapes **2014**,		5
96	Test data analytics Exploring spatial and test-item correlations in production test data **2013**,		12
95	Towards data reliable crossbar-based memristive memories **2013**,		22
94	Digital-to-analog and analog-to-digital conversion with metal oxide memristors for ultra-low power computing **2013**,		25

93	Energy and Performance Characterization of Mobile Heterogeneous Computing **2012**,		2
92	On error modeling of electrical bugs for post-silicon timing validation **2012**,		3
91	Power-Efficient Calibration and Reconfiguration for Optical Network-on-Chip. *Journal of Optical Communications and Networking*, **2012**, 4, 955	4.1	20
90	Comprehensive online defect diagnosis in on-chip networks **2012**,		35
89	Power-efficient calibration and reconfiguration for on-chip optical communication **2012**,		1
88	Platform characterization for Domain-Specific Computing **2012**,		12
87	End-to-end error correction and online diagnosis for on-chip networks **2011**,		45
86	Organic Pseudo-CMOS Circuits for Low-Voltage Large-Gain High-Speed Operation. *IEEE Electron Device Letters*, **2011**, 32, 1448-1450	4.4	48
85	Time-Multiplexed Online Checking. *IEEE Transactions on Computers*, **2011**, 60, 1300-1312	2.5	9
84	Pseudo-CMOS: A Design Style for Low-Cost and Robust Flexible Electronics. *IEEE Transactions on Electron Devices*, **2011**, 58, 141-150	2.9	162
83	Post-silicon bug detection for variation induced electrical bugs **2011**,		2
82	GPU-accelerated fault simulation and its new applications **2011**,		8
81	Energy-optimized mapping of application to smartphone platform □A case study of mobile face recognition **2011**,		11
80	Pseudo-CMOS: A novel design style for flexible electronics **2010**,		7
79	Calibration-assisted production testing for digitally-calibrated ADCs **2010**,		1
78	nGFSIM : A GPU-based fault simulator for 1-to-n detection and its applications **2010**,		16
77	A case study of Time-Multiplexed Assertion Checking for post-silicon debugging **2010**,		2
76	Recent Advances in Analog, Mixed-Signal, and RF Testing. *IPSJ Transactions on System LSI Design Methodology*, **2010**, 3, 19-46	0.2	14

75	Signature-Based Testing for Digitally-Assisted Adaptive Equalizers in High-Speed Serial Links **2009**,		4
74	Yield and Cost Analysis of a Reliable NoC **2009**,		23
73	Design for Low Power and Reliable Flexible Electronics: Self-Tunable Cell-Library Design. *Journal of Display Technology*, **2009**, 5, 206-215		36
72	TAC: Testing time reduction for digitally-calibrated designs **2009**,		1
71	A Built-in self-calibration scheme for pipelined ADCs **2009**,		9
70	Low Overhead Time-Multiplexed Online Checking: A Case Study of An H.264 Decoder **2009**,		1
69	Bit-Error Rate Estimation for Bang-Bang Clock and Data Recovery Circuit in High-Speed Serial Links **2008**,		4
68	A Cost Analysis Framework for Multi-core Systems with Spares **2008**,		20
67	Digitally-Assisted Analog/RF Testing for Mixed-Signal SoCs **2008**,		8
66	A Clock-Less Jitter Spectral Analysis Technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2008**, 55, 2263-2272	3.9	4
65	Testable Design for Advanced Serial-Link Transceivers **2007**,		2
64	An Efficient Diagnostic Test Pattern Generation Framework Using Boolean Satisfiability **2007**,		16
63	An Accurate Jitter Estimation Technique for Efficient High Speed I/O Testing **2007**,		6
62	Silicon Debug for Timing Errors. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2007**, 26, 2084-2088	2.5	1
61	Bit-Error-Rate Estimation for High-Speed Serial Links. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2006**, 53, 2616-2627	3.9	9
60	Simulation-Based Functional Test Generation for Embedded Processors. *IEEE Transactions on Computers*, **2006**, 55, 1335-1343	2.5	25
59	Learning a sparse, corner-based representation for time-varying background modelling **2005**,		1
58	A new sigma-delta modulator architecture for testing using digital stimulus. *IEEE Transactions on Circuits and Systems Part 1: Regular Papers*, **2004**, 51, 206-213		14

57	Self-referential verification for gate-level implementations of arithmetic circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 1102-1112	2.5	2
56	Critical path selection for delay fault testing based upon a statistical timing model. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2004**, 23, 1550-1565	2.5	60
55	Enhanced Symbolic Simulation for Functional Verification of Embedded Array Systems. *Design Automation for Embedded Systems*, **2003**, 8, 173-188	0.6	
54	Modeling, testing, and analysis for delay defects and noise effects in deep submicron devices. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2003**, 22, 756-769	2.5	44
53	Practical considerations in applying /spl Sigma/-/spl Delta/ modulation-based analog BIST to sampled-data systems. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **2003**, 50, 553-566		17
52	False-path-aware statistical timing analysis and efficient path selection for delay testing and timing validation **2002**,		65
51	Self-referential verification of gate-level implementations of arithmetic circuits **2002**,		3
50	Using word-level ATPG and modular arithmetic constraint-solving techniques for assertion property checking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2001**, 20, 381-391	2.5	27
49	Limitations and challenges of computer-aided design technology for CMOS VLSI. *Proceedings of the IEEE*, **2001**, 89, 341-365	14.3	35
48	On improving test quality of scan-based BIST. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2000**, 19, 928-938	2.5	19
47	Test generation for linear time-invariant analog circuits. *IEEE Transactions on Circuits and Systems Part 2: Express Briefs*, **1999**, 46, 554-564		21
46	ErrorTracer: design error diagnosis based on fault simulation techniques. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1999**, 18, 1341-1352	2.5	19
45	AutoFix: a hybrid tool for automatic logic rectification. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1999**, 18, 1376-1384	2.5	11
44	Fault emulation: A new methodology for fault grading. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1999**, 18, 1487-1495	2.5	59
43	Efficient test-point selection for scan-based BIST. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **1998**, 6, 667-676	2.6	12
42	A hybrid methodology for switching activities estimation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1998**, 17, 357-366	2.5	3
41	Postlayout logic restructuring using alternative wires. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1997**, 16, 587-596	2.5	29
40	Pseudorandom testing for mixed-signal circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1997**, 16, 1173-1185	2.5	35

39	Resynthesis of Combinational Circuits for Path Count Reduction and for Path Delay Fault Testability. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **1997**, 11, 43-54	0.7	4
38	Generation of high quality tests for robustly untestable path delay faults. *IEEE Transactions on Computers*, **1996**, 45, 1379-1392	2.5	30
37	Perturb and simplify: multilevel Boolean network optimizer. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **1996**, 15, 1494-1504	2.5	47
36	Fault macromodeling and a testing strategy for opamps. *Journal of Electronic Testing: Theory and Applications (JETTA)*, **1996**, 9, 225-235	0.7	6
35	Analog fault diagnosis for unpowered circuit boards		2
34	Vector Generation For Maximum Instantaneous Current Through Supply Lines For CMOS Circuits		30
33	Design for primitive delay fault testability		1
32	ErrorTracer: a fault simulation-based approach to design error diagnosis		13
31	Post-layout Logic Restructuring For Performance Optimization		7
30	AQUILA: An equivalence verifier for large sequential circuits		11
29	Exact and approximate estimation for maximum instantaneous current of CMOS circuits		3
28	Production-oriented interface testing for PCI-Express by enhanced loop-back technique		4
27	Fast Human Detection Using a Cascade of Histograms of Oriented Gradients		209
26	BER estimation for serial links based on jitter spectrum and clock recovery characteristics		4
25	Adaptive learning of an accurate skin-color model		3
24	A circuit SAT solver with signal correlation guided learning		15
23	Induction-based gate-level verification of multipliers		2
22	Self-testing second-order delta-sigma modulators using digital stimulus		2

21	On theoretical and practical considerations of path selection for delay fault testing	9
20	Path selection for delay testing of deep sub-micron devices using statistical performance sensitivity analysis	20
19	A BIST scheme for on-chip ADC and DAC testing	29
18	Characterization of a pseudo-random testing technique for analog and mixed-signal built-in-self-test	8
17	Testing and characterization of the one-bit first-order delta-sigma modulator for on-chip analog signal analysis	4
16	Estimation of maximum power supply noise for deep sub-micron designs	5
15	Delay testing considering power supply noise effects	19
14	Specification back-propagation and its application to DC fault simulation for analog/mixed-signal circuits	9
13	Analysis of performance impact caused by power supply noise in deep submicron devices	25
12	Testing high speed VLSI devices using slower testers	5
11	Fault emulation: a new approach to fault grading	1
10	Generation of high quality tests for functional sensitizable paths	10
9	Speeding up power estimation by topological analysis	5
8	Minimax end-to-end delay routing and capacity assignment for virtual circuit networks	3
7	Identification and test generation for primitive faults	16
6	A new hybrid methodology for power estimation	3
5	An ATPG-based framework for verifying sequential equivalence	1
4	On verifying the correctness of retimed circuits	8

List of Publications

3	A Comprehensive Fault Macromodel For Opamps	1
2	An Accurate Jitter Estimation Technique for Efficient High Speed I/O Testing	3
1	Fault macromodeling for analog/mixed-signal circuits	3