Suchismita Tewari

List of Publications by Year
in descending order

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		1307594	1125743
21	168	7	13
papers	citations	h-index	g-index

21	21	21	86
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Enhancement of pH-sensitivity using In0.53Ga0.47As channel ion-sensitive-field-effect-transistors. Microsystem Technologies, 2022, 28, 659-664.	2.0	1
2	Asymmetric-Elevated-Source-Drain TFET: A Fairly Scalable and Reliable Device Architecture for Sub-400-mV Low-Stand-by-Power Digital Applications. IETE Technical Review (Institution of Electronics) Tj ETQq0 0 0 rgBT /Overlock 10 T	2.2	8
3	Architecture- and Gate-Oxide-Level Optimization of a Si-Based Asymmetric U-TFET for Low Power Operation: a Real-Time Gate/Drain Electrostatic Based Leakage Perspective. Silicon, 2022, 14, 10719-10727.	3.3	1
4	Dual-Metal Double-Gate with Low-k/High-k Oxide Stack Junctionless MOSFET for a Wide Range of Protein Detection: a Fully Electrostatic Based Numerical Approach. Silicon, 2021, 13, 441-450.	3.3	15
5	High-Performance pH Sensors Using Ion-Sensitive InGaAs-Channel MOSFETs at Sub-100Ânm Technology Node. Journal of Electronic Materials, 2021, 50, 1292-1300.	2.2	3
6	Role of Corner-Effect and Channel Epilayer Thickness on the Performance of a Unique pTFET-Based Biosensor (epiCOR-pTFET-Biosensor) Device in Sub-100-nm Gate Length. IEEE Nanotechnology Magazine, 2021, 20, 678-686.	2.0	1
7	Comparative Study of Logic Performance of Hybrid CMOSFETs at Deca-Nanometer Regime. Lecture Notes in Electrical Engineering, 2021, , 459-467.	0.4	0
8	Impact of sidewall spacer on n-InGaAs devices and hybrid InGaAs/Si CMOS amplifiers in deca-nanometer regime. Microsystem Technologies, 2020, 26, 3077-3084.	2.0	3
9	Impact of aspect ratio of nanoscale hybrid p-Ge/n-Si complementary FinFETs on the logic performance. Microsystem Technologies, 2020, 26, 3069-3076.	2.0	2
10	Negative bias temperature instability (NBTI) effects on p-Si/n-InGaAs hybrid CMOSFETs for digital applications. Microsystem Technologies, 2020, 26, 1173-1178.	2.0	2
11	Optimization of Hetero-Gate-Dielectric Tunnel FET for Label-Free Detection and Identification of Biomolecules. IEEE Transactions on Electron Devices, 2020, 67, 2157-2164.	3.0	21
12	Exploring p-channel TFET for Optimum Cavity-Length Window in Detecting a Wide Variety of Protein-Molecules with the Effect of Their Position Dependent Variability on Sensitivity. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2020, , 1-10.	3.2	3
13	Impact of channel thickness and spacer length on logic performance of p-Ge/n-Si hybrid CMOSFETs for ULSI applications. Superlattices and Microstructures, 2017, 109, 316-323.	3.1	2
14	Impact of a Spacer Layer on the Analog Performance of Asymmetric InP/InGaAs nMOSFETs. IEEE Transactions on Electron Devices, 2016, 63, 2313-2320.	3.0	20
15	Performance of CMOS With Si pMOS and Asymmetric InP/InGaAs nMOS for Analog Circuit Applications. IEEE Transactions on Electron Devices, 2015, 62, 1655-1658.	3.0	8
16	Investigation on High-Performance CMOS With p-Ge and n-InGaAs MOSFETs for Logic Applications. IEEE Nanotechnology Magazine, 2015, 14, 275-281.	2.0	17
17	Effects of channel barrier layer on the analog performance of p-Ge/ n-InGaAs CMOS devices. , 2014, , .		0
18	EFFECTS OF A BARRIER LAYER IN INGAAS CHANNEL MOSFETS FOR ANALOG/ MIXED SIGNAL SYSTEM-ON-CHIP APPLICATIONS. International Journal of Electrical and Electronics Engineering, 2014, , 281-284.	0.1	0

#	Article	IF	Citations
19	Impact of Different Barrier Layers and Indium Content of the Channel on the Analog Performance of InGaAs MOSFETs. IEEE Transactions on Electron Devices, 2013, 60, 1584-1589.	3.0	29
20	Analog performance of dual-material gate InGaAs MOSFETs. , 2012, , .		0
21	Study of InGaAs-Channel MOSFETs for Analog/Mixed-Signal System-on-Chip Applications. IEEE Electron Device Letters, 2012, 33, 372-374.	3.9	37