Shen-Iuan Liu

List of Publications by Year
in descending order

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249 papers	4,586 citations	126708 33 h-index	149479 56 g-index
249 all docs	249 docs citations	249 times ranked	2175 citing authors

#	Article	IF	Citations
1	A Wide-Range FD for Referenceless Baud-Rate CDR Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 60-64.	2.2	3
2	A Low-Jitter Sub-Sampling PLL With a Sub-Sampling DLL. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 269-273.	2.2	5
3	A 20-Gb/s Jitter-Tolerance-Enhanced Digital CDR With One-Tap DFE. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 894-898.	2.2	0
4	A 2â€“3 GHz Fast-Locking PLL Using Phase Error Compensator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2026-2030.	2.2	1
5	A 0.0067-mm² 12-bit 20-MS/s SAR ADC Using Digital Place-and-Route Tools in 40-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 905-914.	2.1	6
6	An Adaptive Digital PLL Based on BBPFD Transition Probability. , 2022, , .		0
7	An Injection-Locked Clock Multiplier With Injection Strength Calibration. , 2022, , .		0
8	A 5-Gb/s Adaptive Digital CDR Circuit With SSC Capability and Enhanced High-Frequency Jitter Tolerance. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 161-165.	2.2	5
9	A Type-I PLL With Foreground Loop Bandwidth Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1103-1107.	2.2	1
10	A 2.4â€“3.0GHz Process-Tolerant Sub-Sampling PLL With Loop Bandwidth Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 873-877.	2.2	3
11	A 10.4â€“16-Gb/s Reference-Less Baud-Rate Digital CDR With One-Tap DFE Using a Wide-Range FD. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 4566-4575.	3.5	2
12	An Adaptive Loop Gain Tracking Digital PLL Using Spectrum-Balancing Technique. , 2021, , .		3
13	A Digital Phase-Locked Loop With Background Supply Noise Cancellation. , 2021, , .		0
14	High-Q Support Transducer MEMS Resonators Enabled Low-Phase-Noise Oscillators. IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control, 2021, 68, 1387-1398.	1.7	11
15	A Jitter-Tolerance-Enhanced Digital CDR Circuit Using Background Loop Gain Controller. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1837-1841.	2.2	0
16	A 13.56 MHz Current-Mode Wireless Power Receiver With Energy-Investment Capability. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 205-209.	2.2	2
17	A 500nW-50Î¼ W Indoor Photovoltaic Energy Harvester with Multi-mode MPPT. , 2020, , .		1
18	A 2.4-GHz Area-Efficient and Fast-Locking Subharmonically Injection-Locked Type-I PLL. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2474-2478.	2.1	10

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19	A 64-Gb/s PAM-4 Optical Receiver With Amplitude/Phase Correction and Threshold Voltage/Data Level Calibration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1726-1735.	2.1	6
20	An Indoor Photovoltaic Energy Harvester Using Time-Based MPPT and On-Chip Photovoltaic Cell. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2432-2436.	2.2	17
21	A 1.22 mW 2.4 GHz PLL Using a Single-Ring-Oscillator-Based Integrator With Background Frequency Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2169-2179.	3.5	4
22	A PVT-Tolerant Injection-Locked Clock Multiplier With a Frequency Calibrator Using a Delay Time Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 177-181.	2.2	4
23	A PVT-Tolerant MDLL Using a Frequency Calibrator and a Voltage Monitor. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 2698-2702.	2.1	4
24	A 13.4-MHz Relaxation Oscillator With Temperature Compensation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 1725-1729.	2.1	18
25	A 2.4-GHz Frequency-Drift-Compensated Phase-Locked Loop With 2.43 ppm/Â°C Temperature Coefficient. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 501-510.	2.1	3
26	An On-Chip Relaxation Oscillator With Comparator Delay Compensation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 969-973.	2.1	15
27	A Digital Phase-Locked Loop With Background Supply Voltage Sensitivity Minimization. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1830-1839.	3.5	8
28	A 13.56 MHz 88.7%-PCE Voltage Doubling Rectifier Using Adaptive Delay Time and Pulse-Width Control. , 2018, , .		1
29	A 5 Gb/s Voltage-Mode Transmitter Using Adaptive Time-Based De-Emphasis. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 959-968.	3.5	11
30	A 0.31-pJ/bit 20-Gb/s DFE With 1 Discrete Tap and 2 IIR Filters Feedback in 40-nm-LP CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 1282-1286.	2.2	13
31	A Voltage Multiplier With Adaptive Threshold Voltage Compensation. IEEE Journal of Solid-State Circuits, 2017, 52, 2208-2214.	3.5	25
32	A 2.25â€“2.7 GHz Area-Efficient Subharmonically Injection-Locked Fractional-N Frequency Synthesizer With a Fast-Converging Correlation Loop. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 811-822.	3.5	17
33	A 0.035-pJ/bit/dB 20-Gb/s Adaptive Linear Equalizer With an Adaptation Time of 2.68 $muext{s}$. IEEE Transactions on Circuits and Systems II: Express Briefs, 2017, 64, 645-649.	2.2	7
34	A 56Gbps PAM-4 optical receiver front-end. , 2017, , .		8
35	A digital MDLL using switched biasing technique to reduce low-frequency phase noise. , 2016, , .		0
36	A 10â€“20 Gb/s CDR circuit with 6200ppm frequency tracking. , 2016, , .		0

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37	19.5 A 3.2GHz digital phase-locked loop with background supply-noise cancellation. , 2016, , .		17
38	A 10-bit 40-MS/s Time-Domain Two-Step ADC With Short Calibration Time. IEEE Transactions on Circuits and Systems II: Express Briefs, 2016, 63, 126-130.	2.2	13
39	A 12-bit 3.4 MS/s Two-Step Cyclic Time-Domain ADC in 0.18- CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 1470-1483.	2.1	15
40	A Loop Gain Optimization Technique for Integer-<formula formulatype="inline"><tex Notation="TeX">N</tex></formula> TDC-Based Phase-Locked Loops. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 1873-1882.	3.5	20
41	A digital bang-bang phase-locked loop with bandwidth calibration. , 2015, , .		4
42	A Subharmonically Injection-Locked PLL With Calibrated Injection Pulsewidth. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 548-552.	2.2	28
43	A 0.43pJ/bit true random number generator. , 2014, , .		13
44	A 5–20 Gb/s power scalable adaptive linear equalizer using edge counting. , 2014, , .		3
45	A low-input-swing AC-DC voltage multiplier using Schottky diodes. , 2014, , .		1
46	A 2×25 Gb/s clock and data recovery with background amplitude-locked loop. , 2014, , .		1
47	A 0.3V 10bit 7.3fJ/conversion-step SAR ADC in 0.18μm CMOS. , 2014, , .		5
48	Nanopower CMOS Relaxation Oscillators With Sub-100 <inline-formula> <tex-math notation="TeX">$hbox{ppm}/^{circ}hbox{C}$</tex-math></inline-formula> Temperature Coefficient. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 661-665.	2.2	28
49	A silicon nanowire-based bio-sensing system with digitized outputs for acute myocardial infraction diagnosis. , 2014, , .		0
50	An All-Digital Despreading Clock Generator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 16-20.	2.2	1
51	A Wide-Range PLL Using Self-Healing Prescaler/VCO in 65-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 250-258.	2.1	9
52	An All-Digital Spread-Spectrum Clock Generator With Self-Calibrated Bandwidth. IEEE Transactions on Circuits and Systems I: Regular Papers, 2013, 60, 2813-2822.	3.5	5
53	A Current-Reused Injection-Locked Frequency Multiplication/Division Circuit in 40-nm CMOS. IEEE Transactions on Microwave Theory and Techniques, 2013, 61, 1523-1532.	2.9	26
54	A 4.8-GHz Dividerless Subharmonically Injection-Locked All-Digital PLL With a FOM of $-$252.5 dB. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 547-551.	2.2	17

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55	A 7.5-Gb/s One-Tap-FFE Transmitter With Adaptive Far-End Crosstalk Cancellation Using Duty Cycle Detection. IEEE Journal of Solid-State Circuits, 2013, 48, 391-404.	3.5	20
56	Ultrasonic telemetry and neural stimulator with FSK-PWM signaling. , 2013, , .		1
57	Ultrasonic Power/Data Telemetry and Neural Stimulator With OOK-PM Signaling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 827-831.	2.2	21
58	4-Gb/s Parallel Receivers With Adaptive FEXT Cancellation by Pulse Width and Amplitude Calibrations. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 622-626.	2.2	1
59	A Submicrowatt 1.1-MHz CMOS Relaxation Oscillator With Temperature Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 837-841.	2.2	51
60	Divide-by-Three Injection-Locked Frequency Dividers Over 200 GHz in 40-nm CMOS. IEEE Journal of Solid-State Circuits, 2013, 48, 405-416.	3.5	7
61	A 2.4-GHz Subharmonically Injection-Locked PLL With Self-Calibrated Injection Timing. IEEE Journal of Solid-State Circuits, 2013, 48, 417-428.	3.5	62
62	A 10-Gb/s Adaptive Parallel Receiver With Joint XTC and DFE Using Power Detection. IEEE Journal of Solid-State Circuits, 2013, 48, 2815-2826.	3.5	11
63	A 300 GHz Divide-by-2 ILFD Using Frequency Boosting Technique. IEEE Microwave and Wireless Components Letters, 2013, 23, 599-601.	2.0	6
64	4-Gb/s Parallel Receivers With Adaptive Far-End Crosstalk Cancellation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 252-256.	2.2	3
65	G-Band Injection-Locked Frequency Dividers Using pi-type LC Networks. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 315-323.	3.5	7
66	A Leakage-Current-Recycling Phase-Locked Loop in 65 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2012, 47, 2693-2700.	3.5	10
67	A 20Gb/s adaptive duobinary transceiver. , 2012, , .		1
68	A 6-GHz All-Digital Fractional-N Frequency Synthesizer Using FIR-Embedded Noise Filtering Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 267-271.	2.2	6
69	Inductorless Wideband CMOS Low-Noise Amplifiers Using Noise-Canceling Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2012, 59, 305-314.	3.5	108
70	A 3.6 mW 125.7â€“131.9 GHz Divide-by-4 Injection-Locked Frequency Divider in 90 nm CMOS. IEEE Microwave and Wireless Components Letters, 2012, 22, 132-134.	2.0	30
71	A 104-GHz Phase-Locked Loop Using a VCO at Second Pole Frequency. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 80-88.	2.1	25
72	A fast-locking phase-locked loop using CP control and gated VCO. , 2012, , .		2

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73	An All-Digital Jitter Tolerance Measurement Technique for CDR Circuits. IEEE Transactions on Circuits and Systems II: Express Briefs, 2012, 59, 148-152.	2.2	16
74	3.6mW D-band divide-by-3 injection-locked frequency dividers in 65nm CMOS. , 2011, , .		6
75	A Rail-to-Rail Class-B Buffer With DC Level-Shifting Current Mirror and Distributed Miller Compensation for LCD Column Drivers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 1761-1772.	3.5	21
76	A leakage-current-recycling phase-locked loop in 65nm CMOS technology. , 2011, , .		2
77	Analysis and Design of D-Band Injection-Locked Frequency Dividers. IEEE Journal of Solid-State Circuits, 2011, 46, 1250-1264.	3.5	34
78	A 132.6-GHz Phase-Locked Loop in 65 nm Digital CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 617-621.	2.2	8
79	A Digitally-Calibrated Phase-Locked Loop With Supply Sensitivity Suppression. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 592-602.	2.1	12
80	A 1â€“16-Gb/s Wide-Range Clock/Data Recovery Circuit With a Bidirectional Frequency Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 487-491.	2.2	20
81	A Noise Filtering Technique for Fractional-N Frequency Synthesizers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 139-143.	2.2	10
82	A 40-GHz Fast-Locked All-Digital Phase-Locked Loop Using a Modified Bang-Bang Algorithm. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 321-325.	2.2	42
83	Decision Feedback Equalizers Using the Back-Gate Feedback Technique. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 897-901.	2.2	4
84	Design of a CMOS low-power and low-voltage four-quadrant analog multiplier. Analog Integrated Circuits and Signal Processing, 2010, 63, 307-312.	0.9	23
85	A 35.56GHz all-digital phase-locked loop with high resolution varactors. , 2010, , .		2
86	A 20-Gb/s Transmitter With Adaptive Preemphasis in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 319-323.	2.2	18
87	An integrating analog-to-digital data converter with variable resolution. , 2010, , .		0
88	A 1.62/2.7-Gb/s Adaptive Transmitter With Two-Tap Preemphasis Using a Propagation-Time Detector. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 178-182.	2.2	10
89	A 10-MS/s-to-100-kS/s Power-Scalable Fully Differential CBSC 10-Bit Pipelined ADC With Adaptive Biasing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 11-15.	2.2	16
90	A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial-Link Receivers. IEEE Journal of Solid-State Circuits, 2010, 45, 433-446.	3.5	5

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91	A Phase-Locked Loop With Background Leakage Current Compensation. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 666-670.	2.2	6
92	A 198.9GHz-to-201.0GHz injection-locked frequency divider in 65nm CMOS. , 2010, , .		5
93	A 10Gb/s inductorless quarter-rate clock and data recovery circuit in 0.13um CMOS. , 2009, , .		3
94	A CBSC second-order sigma-delta modulator in 3μm LTPS-TFT technology. , 2009, , .		11
95	Effects of hydration levels on the bandwidth of microwave resonant absorption induced by confined acoustic vibrations. Applied Physics Letters, 2009, 95, .	1.5	13
96	A wireless power telemetry with self-calibrated resonant frequency. , 2009, , .		0
97	Microwave resonant absorption of viruses through dipolar coupling with confined acoustic vibrations. Applied Physics Letters, 2009, 94, .	1.5	42
98	A 140MS/s 10-bit pipelined ADC with a folded S/H stage. , 2009, , .		1
99	An 8-bit 20-MS/s ZCBC Time-Domain Analog-to-Digital Data Converter. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 545-549.	2.2	15
100	A 20-MHz to 3-GHz Wide-Range Multiphase Delay-Locked Loop. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 850-854.	2.2	20
101	A 104- to 112.8-GHz CMOS Injection-Locked Frequency Divider. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 555-559.	2.2	10
102	A Leakage-Compensated PLL in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 525-529.	2.2	19
103	Comments on "A 10-Gb/s Inductorless CMOS Analog Equalizer With an Interleaved Active Feedback Topology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 519-519.	2.2	0
104	A Fully Differential Comparator-Based Switched-Capacitor $DeltaSigma$ Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 369-373.	2.2	44
105	A Single-PLL UWB Frequency Synthesizer Using Multiphase Coupled Ring Oscillator and Current-Reused Multiplier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 107-111.	2.2	6
106	A 10-Gb/s Inductorless CMOS Analog Equalizer With an Interleaved Active Feedback Topology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 97-101.	2.2	12
107	A Phase-Locked Loop With Self-Calibrated Charge Pumps in 3-$muhbox{m}$ LTPS-TFT Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 142-146.	2.2	7
108	Loop latency reduction technique for all-digital clock and data recovery circuits. , 2009, , .		7

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109	A frequency synthesizer for Mode-1 MB-OFDM UWB applications. , 2009, , .		3
110	A 50-Gb/s 10-mW Analog Equalizer Using Transformer Feedback Technique in 65-nm CMOS Technology. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 783-787.	2.2	1
111	A delay-locked loop with digital background calibration. , 2009, , .		4
112	An all-digital clock generator for dynamic frequency scaling. , 2009, , .		5
113	A 33.6-to-33.8 Gb/s Burst-Mode CDR in 90 nm CMOS Technology. IEEE Journal of Solid-State Circuits, 2009, 44, 775-783.	3.5	6
114	A 1.5 GHz All-Digital Spread-Spectrum Clock Generator. IEEE Journal of Solid-State Circuits, 2009, 44, 3111-3119.	3.5	54
115	A Digital Calibration Technique for Charge Pumps in Phase-Locked Systems. IEEE Journal of Solid-State Circuits, 2008, 43, 390-398.	3.5	87
116	A 50.8â€“53-GHz Clock Generator Using a Harmonic-Locked PD in 0.13-mum CMOS. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 404-408.	2.2	5
117	A 4-bit 10GSample/sec flash ADC with merged interpolation and reference voltage. , 2008, , .		2
118	40 Gb/s Transimpedance-AGC Amplifier and CDR Circuit for Broadband Data Receivers in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2008, 43, 642-655.	3.5	98
119	An Infinite Phase Shift Delay-Locked Loop With Voltage-Controlled Sawtooth Delay Line. IEEE Journal of Solid-State Circuits, 2008, 43, 2413-2421.	3.5	19
120	A 40 Gb/s CMOS Serial-Link Receiver With Adaptive Equalization and Clock/Data Recovery. IEEE Journal of Solid-State Circuits, 2008, 43, 2492-2502.	3.5	47
121	A Jitter-Tolerance-Enhanced CDR Using a GDCO-Based Phase Detector. IEEE Journal of Solid-State Circuits, 2008, 43, 1217-1226.	3.5	10
122	Full-Rate Bang-Bang Phase/Frequency Detectors for Unilateral Continuous-Rate CDRs. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1214-1218.	2.2	23
123	A dual-band 61.4∼63GHz/75.5∼77.5GHz CMOS receiver in a 90nm technology. , 2008, , .		4
124	An All-Digital Fast-Locking Programmable DLL-Based Clock Generator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 361-369.	3.5	29
125	10-Gb/s Inductorless CDRs With Digital Frequency Calibration. IEEE Transactions on Circuits and Systems I: Regular Papers, 2008, 55, 2514-2524.	3.5	11
126	A sub-1v low-dropout regulator with an on-chip voltage reference. , 2008, , .		2

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127	A 57.1–59GHz CMOS fractional-N frequency synthesizer using quantization noise shifting technique. , 2008, , .		0
128	Frequency dividers with enhanced locking range. , 2008, , .		4
129	A Delay-Locked Loop With Statistical Background Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 961-965.	2.2	7
130	A 15–20GHz delay-locked loop in 90nm CMOS technology. , 2008, , .		1
131	A 62–66.1GHz phase-locked loop in 0.13um CMOS technology. , 2008, , .		0
132	A 3â€“8 GHz Delay-Locked Loop With Cycle Jitter Calibration. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 1094-1098.	2.2	12
133	A 40Gb/s low-power analog equalizer in 0.13μm CMOS technology. , 2008, , .		1
134	A merged CMOS digital near-end crosstalk canceller and analog equalizer for multi-lane serial-link receivers. , 2008, , .		0
135	A 40GHz fractional-n frequency synthesizer in 0.13μm CMOS. , 2008, , .		1
136	A 0.18-$mu{hbox {m}}$ CMOS 1.25-Gbps Automatic-Gain-Control Amplifier. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 136-140.	2.2	29
137	A 4-54GHz Static Frequency Divider with Back-Gate Coupling. , 2007, , .		5
138	A 4-Bit, 13.5GSample/sec Track-and-Hold Circuit. , 2007, , .		1
139	A 2.4GHz Efficiency-Enhanced Rectifier for Wireless Telemetry. , 2007, , .		5
140	A 1V 5-Bit 5GSample/sec CMOS ADC for UWB Receivers. , 2007, , .		12
141	A Broadband Noise-Canceling CMOS LNA for 3.1â€“10.6-GHz UWB Receivers. IEEE Journal of Solid-State Circuits, 2007, 42, 329-339.	3.5	325
142	A 0.5â€“5-GHz Wide-Range Multiphase DLL With a Calibrated Charge Pump. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 939-943.	2.2	43
143	A 40â€“550 MHz Harmonic-Free All-Digital Delay-Locked Loop Using a Variable SAR Algorithm. IEEE Journal of Solid-State Circuits, 2007, 42, 361-373.	3.5	132
144	A 1.2-V 37â€“38.5-GHz Eight-Phase Clock Generator in 0.13-mum CMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 1261-1270.	3.5	33

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145	A 2.5 GHz All-Digital Delay-Locked Loop in 0.13 $mu{hbox {m}}$ CMOS Technology. IEEE Journal of Solid-State Circuits, 2007, 42, 2338-2347.	3.5	67
146	An Ultra-Wide-Band 0.4–10-GHz LNA in 0.18-<formula formulatype="inline"><tex>mu</tex></formula>m CMOS. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 217-221.	2.3	140
147	A 7-BIT 400MS/s sub-ranging flash ADC in 0.18um CMOS. , 2007, , .		4
148	A 8-bit 14OMS/s Pipelined ADC Using Folded Sample-and-Hold Stage. , 2007, , .		3
149	A 62.5–625-MHz Anti-Reset All-Digital Delay-Locked Loop. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 566-570.	2.3	23
150	An infinite phase shift delay-locked loop with voltage-controlled sawtooth delay line. , 2007, , .		0
151	A 10-BIT 100MS/s pipelined ADC IN 0.18μm CMOS technology. , 2007, , .		1
152	A Low-Jitter Spread Spectrum Clock Generator Using FDMP. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 979-983.	2.2	22
153	A Time-Constant Calibrated Phase-Locked Loop With a Fast-Locked Time. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 34-37.	2.3	8
154	A 39.2~45.5GHz Frequency Divider Using a Switched Cross-Coupled Pair. , 2007, , .		0
155	An all-digital reused-SAR delay-locked loop with adjustable duty cycle. , 2007, , .		2
156	A DLL-Based Variable-Phase Clock Buffer. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 1072-1076.	2.2	6
157	Spur-Suppression Techniques for Frequency Synthesizers. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2007, 54, 653-657.	2.3	29
158	A Half-Rate Bang-Bang Phase/Frequency Detector for Continuous-Rate CDR Circuits. , 2007, , .		5
159	A Wide-Range All-Digital Duty Cycle Corrector with a Period Monitor. , 2007, , .		12
160	A passive filter for 10-Gb/s analog equalizer in 0.18-μm CMOS technology. , 2007, , .		0
161	A 10Gb/s burst-mode transimpedance amplifier in 0.13μm CMOS. , 2007, , .		0
162	A 44GHz Dual-Modulus Divide-by-4/5 Prescaler in 90nm CMOS Technology. , 2006, , .		9

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163	A 10Gbps Burst-Mode CDR Circuit in 0.18Î¼m CMOS. , 2006, , .		11
164	A 0.7â€“2-GHz Self-Calibrated Multiphase Delay-Locked Loop. IEEE Journal of Solid-State Circuits, 2006, 41, 1051-1061.	3.5	44
165	All-Digital Delay-Locked Loop/Pulsewidth-Control Loop With Adjustable Duty Cycles. IEEE Journal of Solid-State Circuits, 2006, 41, 1262-1274.	3.5	37
166	A 155.52 Mbpsâ€“3.125 Gbps Continuous-Rate Clock and Data Recovery Circuit. IEEE Journal of Solid-State Circuits, 2006, 41, 1380-1390.	3.5	52
167	A 200-Mbps/spl sim/2-Gbps continuous-rate clock-and-data-recovery circuit. IEEE Transactions on Circuits and Systems Part 1: Regular Papers, 2006, 53, 842-847.	0.1	25
168	All-Digital Fast-Locked Synchronous Duty-Cycle Corrector. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1363-1367.	2.3	34
169	A spur-reduction technique for a 5-GHz frequency synthesizer. IEEE Transactions on Circuits and Systems I: Regular Papers, 2006, 53, 526-533.	3.5	46
170	A Fully Integrated Spread Spectrum Clock Generator. , 2006, , .		0
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